CuBrick: A Novel Vertical Dielectric Immersion Cooling Approach for Power Semiconductors

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***Abstract*— This paper presents a novel dielectric immersion cooling concept for power modules using perforated copper blocks, termed "CuBricks," which serve as both heat exchangers and electrical interconnects. Soldered onto a standard FR4 PCB with integrated fluidic pockets, this design eliminates traditional DBC or AMB substrates and enables a vertical coolant flow through the circuit carrier. Focusing exclusively on the thermal characterization of this concept, various single- and double-sided cooled designs are investigated regarding the impact of the channel pattern and copper thickness. Experimental results from a thermal test vehicle are validated against CFD simulations. Finally, a benchmark against dielectric-cooled state-of-the-art research setups and an industrial pin-fin water-glycol-operated automotive power module demonstrates that the CuBrick concept is a promising alternative for high-power-density thermal management, achieving a thermal resistance of down to 0.27 K/W (6.72 mm²K/W) at a pumping power per chip of 0.043 W for a 25 mm² SiC-MOSFET die.**

Keywords— Silicon Carbide (SiC), Power electronics packaging, Thermal management, Immersion cooling, Dielectric cooling, Direct cooling, Thermal resistance

I. Introduction

Immersion cooling of power electronics possesses the potential to revolutionize traditional power module architectures. Direct immersion of the power electronics assembly into a dielectric coolant enables the elimination of traditional insulation and packaging methods, including silicone gel, overmolding and ceramics substrates. From a thermal management standpoint, immersion cooling drastically shortens the thermal path from the semiconductor to the coolant and facilitates double-sided cooling. However, the thermophysical properties of dielectric fluids—typically oil- or ester-based—are inherently inferior to those of water-glycol mixtures. Consequently, novel cooling concepts are required to match or exceed the performance of conventional cooling strategies. Recent research reflects a steadily growing interest in dielectric cooling strategies. In 2018, our group presented a jet impingement approach combined with PCB embedding of IGBTs mounted on thick copper substrates, achieving thermal resistance R_{th} values of 0.52 K/W at a flow rate of 2.5 l/min per IGBT (83 mm²) [1]. In 2022, Moreno [2] presented a concept utilizing slot-jets and skived heat sinks, demonstrating performance comparable to the state-of-the-art pin fin power module within a more compact footprint. In 2023, Chen [3] presented a double-sided oil-cooled power module concept, achieving a 31% reduction in thermal resistance compared to conventionally cooled modules. Furthermore, they evaluated material compatibility by investigating the corrosion behavior of mineral oil- and ester-based coolants on copper, as well as the swelling behavior of rubber O-rings. In 2024, Wang [4] presented a concept for double-sided immersion cooling of power modules utilizing fluorinated dielectric coolants. Among other factors, they investigated different cooling configurations and achieved a 35.6% reduction in chip temperature rise through enhanced thermal management. In 2025, we introduced an approach where SiC-MOSFETs were mounted on copper inlays laminated into a PCB, serving as both electrical interconnects and heat sinks. This design utilized a combination of jet impingement on the bottom side and channel flow on the top side. While this achieved R_{th} values of 0.6 K/W (at a reference pumping power of 0.045 W) comparable to conventional pin-fin cold plates, it did not surpass their performance [5]. Simultaneously, a research group from RWTH Aachen developed a similar modular concept where SiC-MOSFETs were mounted on small (15 x 15 mm) pin-fin coolers, which were soldered to the backside of a PCB [6]. In this setup, the pin-fin coolers also functioned as electrical contacts and heat sinks. This approach was able to outperform conventional reference modules, achieving an R_{th} of 0.52 K/W at comparable pumping power. Additionally, Vethake [7] (2025) presented a DBC-integrated cooler with impressive performance. Although primarily designed for

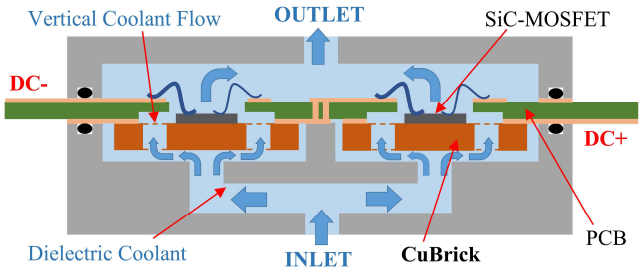


Fig. 1 CuBrick concept with vertical dielectric immersion cooling

Funded by the European Union within the Horizon Europe project "FLAGCHIP" under GA no. 101172794. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or CINEA. Neither the European Union nor the granting authority can be held responsible for them.

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water as coolant, CFD-simulations using dielectric coolants indicated a thermal performance similar to that reported by Kamp [6].

This work proposes the 'CuBrick' concept (Fig. 1), which aims to enhance thermal performance while simultaneously reducing material consumption (i.e., copper volume) through the use of easily fabricable copper heat sinks. This is enabled by a novel vertical coolant flow directed straight through the circuit carrier. The term 'CuBrick' represents the copper block ('Cu') utilized as the heat sink, while introducing this thermal component as a modular building block ('Brick') for power module design. Central to the proposed design is the 'CuBrick' itself—a modular, perforated copper component that functions as both a high-capacity heat exchanger and a high-current interconnect (see Fig. 1). This architecture differs significantly from conventional power module designs. Instead of ceramic substrates, it utilizes a modified FR4-based PCB. Through-hole apertures in the PCB enable a vertical dielectric coolant flow through the circuit carrier and the CuBrick. By positioning the coolant flow in such close proximity to the chips and exploiting the high thermal conductivity of the perforated copper, the design effectively compresses the thermal stack and enhances cooling performance. At the same time, the dielectric liquid replaces the silicone gel used for isolation around the semiconductor chip. The dielectric performance is not within the scope of this paper but studied by our project partner INSA Lyon [8].

This paper is structured as follows: Section II introduces the investigated CuBrick variations and details the dielectric coolant and the thermal test vehicle (TTV) developed for experimental characterization. Section III covers the methodology, focusing on the CFD simulations and the experimental setup. The fabrication steps of the CuBrick boards are presented in Section IV. Subsequently, Section V evaluates and compares the experimental thermal characterization results with the CFD simulations, followed by a benchmark in section VI comparing the CuBrick concept with an industrial reference module and alternative dielectric cooling technologies found in literature. Finally, Section VII concludes the paper with a summary of the key findings and a conclusion.

II. Materials

To investigate the potential of the concept, several CuBrick designs are analysed. This section introduces the design variations, describes the developed thermal test vehicle (TTV) for thermal testing, and details the selected dielectric fluid.

A. CuBrick Variations

The vertical coolant flow, distinctive to the proposed concept, opens new pathways for thermal management using dielectric fluids. To explore these possibilities, several CuBrick variations were designed (see Fig. 2), ranging from single-sided (Design 1, 2) to double-sided cooling configurations (Design 3, 4, 5). In all proposed designs, a SiC-MOSFET is silver sintered onto the underlying CuBrick. This block is maintained at the chip's drain potential and is soldered directly to the PCB. The perforation within the CuBricks is realized through laser-cut slots. This configuration maximizes the effective heat transfer surface area, maintaining the heat spreading capability while minimizing material removal, thereby preserving the thermal mass of the component.

Single-Sided Cooling (Design 1, 2): In these configurations, the gate and source terminals are interconnected via thick Al wire bonds. The through-hole aperture in the PCB directly above the chip is minimized to maximize the surface area available for power trace routing. To ensure an unobstructed coolant flow, a pocket (recess) with a depth of 0.5 mm is machined into the bottom side of the PCB, allowing the coolant to pass from the CuBrick through the circuit carrier without impeding the perforation pattern. Design 1 follows a conservative design route with a 3 mm thick CuBrick and 16 radial slots. In contrast, Design 2 pushes the boundaries of laser-machining capabilities by utilizing a 5 mm CuBrick thickness with parallel slots spaced 1.5 mm apart. All following iterations build upon Design 2 as a foundation to achieve additional gains in performance. The details and dimensions of the individual variations are listed in Table I.

Double-Sided Cooling (Design 3, 4, 5): To further enhance the cooling performance, double-side approaches were evaluated using cost-effective stamped copper parts

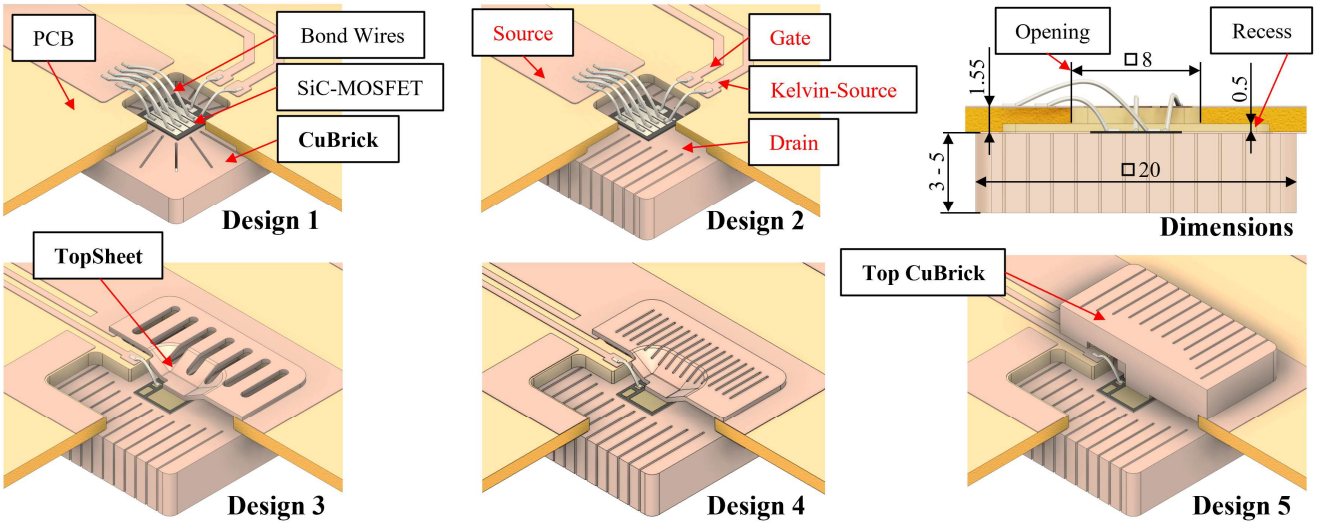


Fig. 2 Investigated CuBrick designs and dimensions

TABLE I
CUBRICK VARIATIONS DESCRIPTION & DIMENSIONS

Design:	Description:	Chips:	CuBrick Dimensions:	Top Contact Dimensions:
1	Single Sided CuBrick (Drain) with Wire Bonds (Source, Gate, Kelvin-Source)	Chip A (29,9 mm²)	Size: 20 x 20 x **3** mm Slots: 0.15 mm (Radial) Count: 16	8x Al Bond Wires (300µm)
2	Single Sided CuBrick (Drain) with Wire Bonds (Source, Gate, Kelvin-Source)			8x Al Bond Wires (300µm)
3	Bottom CuBrick (Drain) with stamped TopSheet (Source, Kelvin-Source) & Wire Bond (Gate)	Chip B (25 mm²)	Size: 20 x 20 x **5** mm Slots: 0.2 mm (Parallel) Pitch: 1.5 mm Count: 24	**TopSheet** Size: 20 x 20 x **0.8** mm Slots: 1 mm Pitch: 2 mm Count: 14 (Parallel)
4	CuBrick (Drain) with hybrid manufactured TopSheet (Source, Kelvin-Source) & Wire Bond (Gate)			**TopSheet** Size: 20 x 20 x **0.8** mm Slots: 0.2 mm Pitch: 1 mm Count: 34 (Parallel)
5	Double CuBrick with bottom CuBrick (Drain), Top CuBrick (Source, Kelvin-Source) & Wire Bond (Gate)			**Top CuBrick** As bottom CuBrick

termed 'TopSheet'. These interconnects can be manufactured either as a stamped-and-bent part with relatively coarse structures (Design 3) or as a hybrid component featuring laser-cut closely spaced slits to further increase the vertical cooling surface area (Design 4). To push the thermal performance to its physical limit, a variation featuring a second CuBrick was examined (Design 5). In this setup, the top CuBrick directly contacts the chip source pad, providing maximum thermal mass and surface area for heat dissipation. The top CuBrick was machined using standard milling to provide sufficient isolation distances to the parts with drain and gate potential.

The actual slot width is determined by the actual post-laser-cutting dimensions, which are detailed in section V (Fabrication) below. It should be noted that different chip types were utilized for the single-sided and double-sided cooling configurations. Design 1, 2 employed chips with Al top metallization compatible with wire bonding. Design 5, however, required different chips featuring a solderable top-side Au-metallization. The specific technical details and geometric parameters of these variations are summarized in Table I. In this work, only Designs 1, 2, and 5 were fabricated and experimentally tested, whereas Designs 3 and 4 were utilized exclusively for CFD simulations.

B. *Thermal Test Vehicle (TTV)*

A Thermal Test Vehicle (TTV), representing a simplified single chip module, was developed to evaluate thermal performance of the concept. It consists of a PCB carrying the CuBrick structure and a housing assembled from 3D-printed plastic components and aluminum top and bottom plates (see Fig. 3). The Housing features inlet and outlet ports screwed into the aluminum plates on opposite sides, enabling a vertical coolant flow. Sealing is ensured by O-rings seated against the PCB. Removable plastic inlays allow the fluidic routing to be flexibly adapted to the various CuBrick designs under investigation. Fig. 3 shows a top and bottom partial cross-sectional view of the developed TTV, along with a detailed view of the parallel slotted CuBrick structure (Design 2) to illustrate the coolant flow. Here the dielectric coolant enters from the bottom, passes through the slots of the CuBrick structure, and converges within the PCB's recess/pocket toward the opening on the top side.

C. *Dielectric Fluid*

The dielectric coolant employed in this study is *Shell EV-Plus TM MIVOLT 808* (formerly *MIVOLT DF7*), a synthetic ester-based fluid specifically engineered for the requirements of the automotive sector [9]. This fluid offers a flash point of 194°C and a low pour point of -75°C. Its relatively low kinematic viscosity is critical for minimizing pressure drops

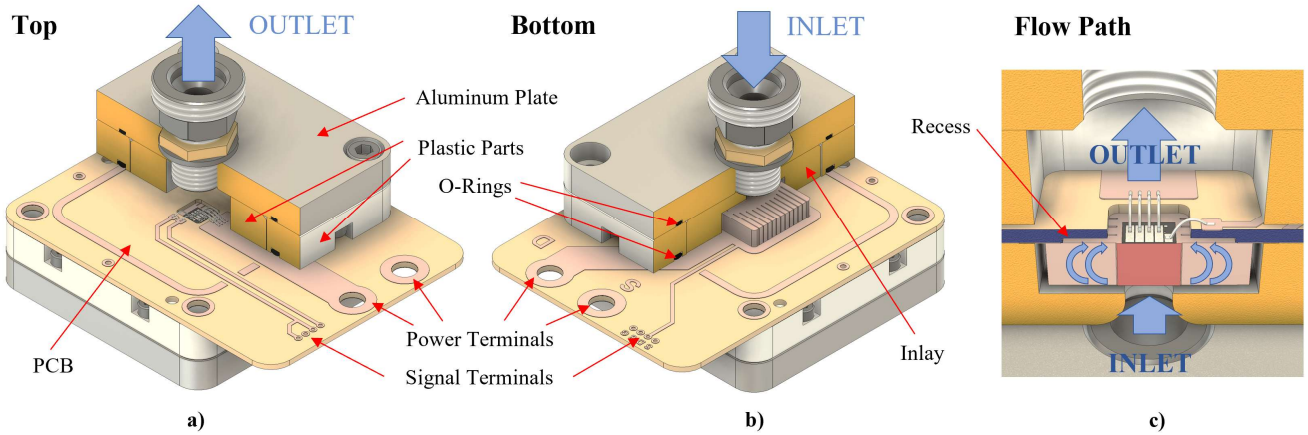


Fig. 3 Thermal Test Vehicle (TTV) partial cross sections a) top view b) bottom view c) flow path visualization

across the slotted CuBrick structure. Furthermore, the fluid is non-toxic and biodegradable, aligning with the sustainability goals of modern power electronic systems. The coolant was tested at 60°C, which represents the standard coolant temperature in automotive applications. The thermal properties of the fluid at this operating point are summarized in Table II.

TABLE II
THERMAL PROPERTIES OF DIELECTRIC COOLANT

Property:	Value (at 60 °C):	Unit:
Density	886	kg/m³
Specific Heat	2.02	kJ/(kg K)
Therm. Conductivity	0.123	W/(m K)
Kinematic Viscosity	4.3	mm²/s

III. METHODOLOGY

This section outlines the applied CFD model and describes the experimental setup used for thermal characterization, providing a detailed insight into both the test apparatus and the corresponding test procedure.

A. CFD-Simulations

To analyse the heat transfer between the SiC-MOSFET to the dielectric coolant, a simplified CFD model was developed using *Ansys Discovery*. To reduce computational effort, half & quarter-models were utilized by exploiting the system's symmetry. The simulation domain was limited to the semiconductor die, the CuBrick, and the dielectric fluid. The mesh was generated using polyhedral elements with five inflation layers and a growth rate of 1.2 to accurately capture boundary layer gradients within the slots (see Fig. 4(a)). Steady-state simulations were performed for coolant flow rates ranging from 0.25 to 3 L/min and a coolant temperature of 60°C. The k-ω shear stress transport (SST) turbulence model was employed. A power dissipation of 200 W was assigned to the chip volume. The junction temperature T_j was determined as the volume average temperature across the chip. The thermophysical properties used for the simulations are summarized in Table III. Prior to conducting the CFD simulations, a mesh sensitivity study was performed to ensure the grid-independence of the numerical results.

TABLE III
MATERIAL PROPERTIES FOR CFD-SIMULATION

Component:	Property:	Value:
CuBrick	Therm. Conductivity	400 W/mK
SiC-MOSFET	Therm. Conductivity	200 W/mK
Ag Sinter Layer	Therm. Conductance	6e6 W/m²K
Solder Layer	Therm. Conductance	5e5 W/m²K

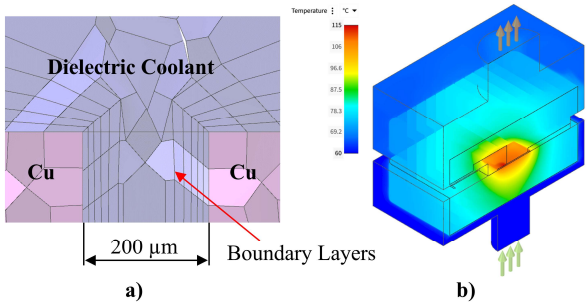


Fig. 4 CFD-Simulation setup showing a) mesh through CuBrick slot b) temperature map of Design 5 model

To quickly assess the flow conditions within the laser-cut slots, the Reynolds number was calculated using the following equation:

$$Re = \frac{w * L}{\nu} = \frac{w * (2h)}{\nu}$$

Where w is the flow velocity through the slot, ν is the kinematic viscosity of the dielectric coolant, and L is the characteristic length. For slot flows, L simplifies to $2h$, where h denotes the slot width. Even at the maximum investigated flow rate of 3 L/min, applied to the design with the fewest slots (Design 1 – radial slots), the resulting Reynolds number is only approximately 500, indicating a purely laminar flow regime within the slot. A CFD simulation utilizing laminar boundary conditions supports this assumption, yielding nearly identical results to those obtained with the *k-ω* SST turbulence model.

IV. EXPERIMENT

The thermal performance of the power modules is characterized by the junction-to-fluid thermal impedance $Z_{th,jf}$ defined as:

$$Z_{th,jf}(t) = \frac{T_j(t) - T_{fluid,inlet}}{P_{loss}}$$

where $T_j(t)$ represents the transient junction temperature following a power loss P_{loss}, and $T_{fluid,inlet}$ is the coolant inlet temperature. The steady-state value of this impedance is referred to as the thermal resistance $R_{th,jf}$. To determine $Z_{th,jf}$, a constant power loss was generated by conducting a regulated load current in the reverse direction through the body diode of the SiC-MOSFET. Upon reaching thermal equilibrium, the load current was disconnected, and the thermal impedance was derived from the cooling transient. The junction temperature was monitored using the body diode voltage of the SiC-MOSFET as a Temperature Sensitive Electrical Parameter (TSEP) at a constant sensing current of 30 mA. An analysis of these and other methods with respect to their measurement uncertainties was conducted by Zhang [10]. Prior to the measurements, a calibration was conducted between 20°C and 130°C, confirming a linear temperature-voltage relationship with a sensitivity of 2.375 mV/K for Chip A (29.9 mm²) and 2.315 mV/K for Chip B (25 mm²) (see Table I). The experimental setup comprised a *Delta SM 18 220* power supply for the load current (with an uncertainty of ± 0.2% of the reading). The source-drain voltage was recorded for 15 sec using a *RIGOL DHO5104* oscilloscope (with a DC gain offset of ± 1% of the reading). Rapid disconnection of the load current was achieved via a custom switching stage based on two MOSFETs. To account for initial oscillations (approx. 50 µs) following the turn-off transient, the maximum junction temperature at t=0 was determined using the square-root-of-time backward interpolation method. Additionally, a moving average filter was applied to the raw data to minimize noise in the resulting $Z_{th,jf}$ curves. The measurements were performed with the dielectric coolant at a temperature of 60°C. Eight different flow rates were investigated ranging from 0.25 to 3 L/min. The flow rate was measured with a *Keyence FD-H10* clamp-on ultrasonic flow sensor on a ¼" pipe with an accuracy of ± 3% down to a flow rate of 2 L/min

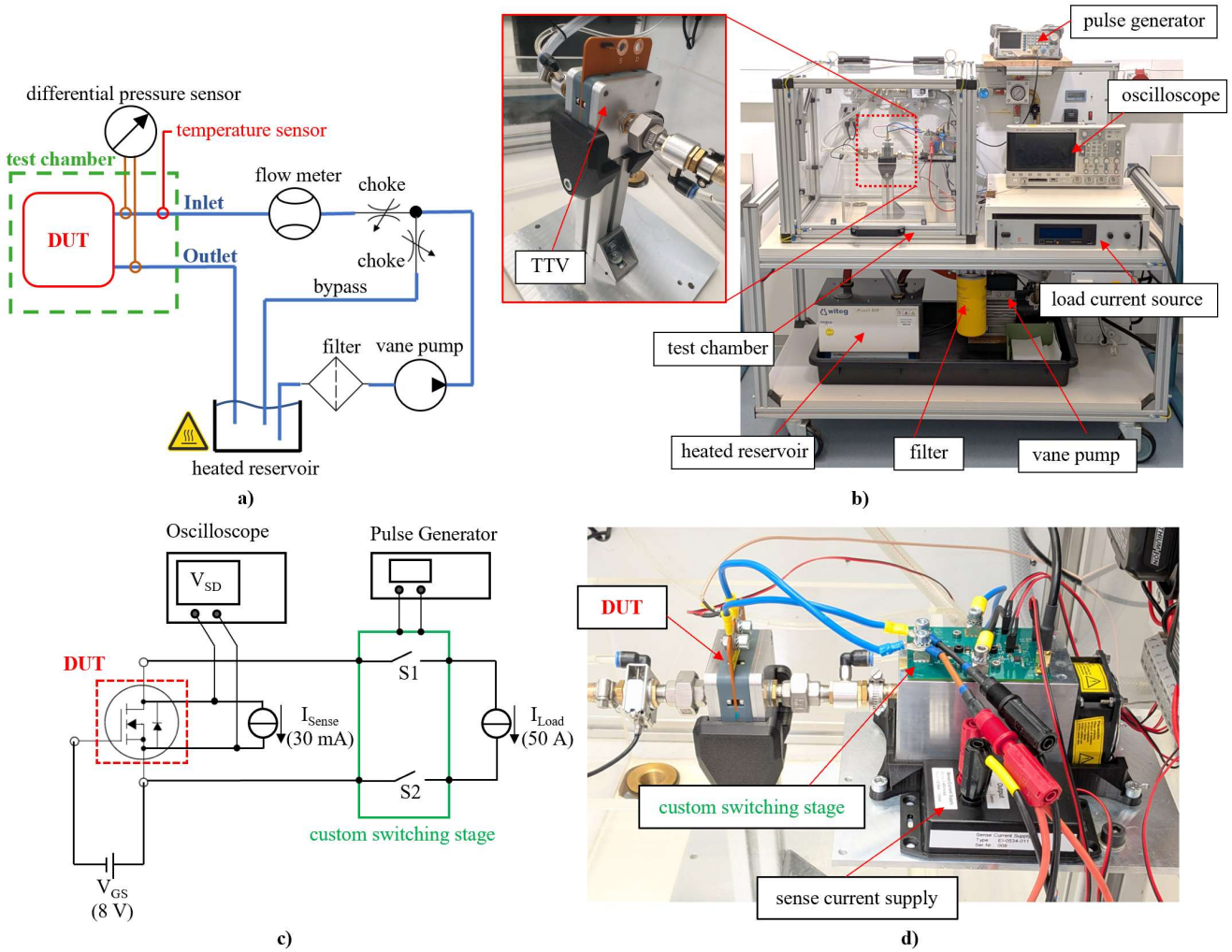


Fig. 5 Test bench a) hydraulic circuit b) test bench with close-up showing the TTV c) electric circuit schematics, and d) DUT connected to switching circuit

and an accuracy of ± 0.06 L/min for lower flow rates. The pressure drop across the TTV was measured with a *Keyence AP-V87WP* differential pressure sensor and two *Keyence AP-12S* probes on inlet and outlet with an accuracy of ± 0.5 %. The coolant inlet temperature was measured with a *Keyence FI-T15* sensor with an accuracy of ± 1.0 °C. Fig. 5 shows the thermal test bench, its hydraulic circuit, and a close-up of the DUT with the custom switching board as well as the corresponding switching circuit. A detailed uncertainty analysis of the entire measurement chain—encompassing the calibration of the SiC semiconductors, the fluid temperature measurement, and the high-resolution measurement of V_{DS} along with its evaluation via a MATLAB script—was conducted, yielding an absolute uncertainty of ± 1.77%. Additionally, to evaluate the repeatability of the R_{th} measurement, a test series of ten consecutive measurements was performed on Design 2 at a repeatedly adjusted flow rate of 1 L/min. This resulted in a standard deviation of 0.00491 K/W and a corresponding random uncertainty of 0.435 %.

V. Fabrication

Standard PCB fabrication techniques were employed to manufacture the two-layer, 1.55 mm thick TTV Board. The process involved drilling the required holes, wet-chemical etching of the 70 µm copper layers using ferric chloride, and mechanically milling the pocket/recess beneath the CuBrick location.

A fiber laser (*Trumpf TruLaser Fiber*) was employed to cut the CuBricks from thick copper sheets. Fig. 6 shows two cross-sectional micrographs of the laser-cut slots for Design 1 (3 mm copper) and Designs 2 & 5 (5 mm copper). It can be observed that the slot geometry differs between the two copper thicknesses, which results from the different laser parameters required. While the slot through the 3 mm copper runs highly parallel with a width of **150** µm due to moderate laser power, the 5 mm copper exhibits distinct inlet and outlet tapers and a wider slot width of **200** µm caused by the necessary higher laser energy input.

To remove sharp edges and solidified copper spatter resulting from the laser process, the components undergo a two-stage treatment. First, both sides are manually ground with sandpaper to achieve a planar surface (see Fig. 7). To

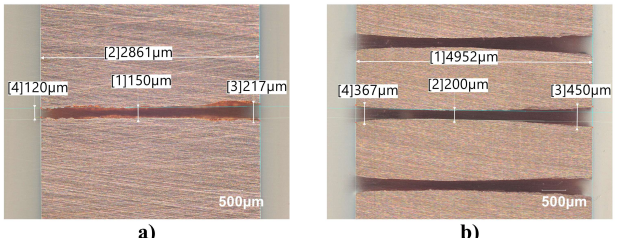


Fig. 6 Micrographs of CuBrick slots for a) Design 1 b) Design 2

clear any copper debris pushed into the slots during grinding, a wet-chemical micro-etching step is introduced. This process also prepares the surface for the subsequent die-attach. The CuBricks are cleaned in an ultrasonic bath with a micro-etch solution at 50°C for about 5 min. Finally, an immersion silver (Ag) finish is applied, completing the preparation for the Ag sintering of the SiC-MOSFETs. Fig. 8 illustrates the fabrication process flow of the constructed CuBrick variants. The silver sintering film, *Alpha Argomax 8020*, is transferred to the backside of the MOSFET dies via a stamping process and subsequently tacked onto the CuBrick structures. Following this pre-assembly, the actual sintering process is conducted using an in-house thermopress tool. To ensure a uniform pressure distribution across the chips, the sintering pressure is applied through a compliant silicone press pad. The CuBrick, with the sintered chip attached, is subsequently integrated onto the PCB with a solder joint. First, solder paste is applied to the PCB using a stencil printing process. To ensure precise positioning of the CuBrick on the PCB, a custom alignment fixture is utilized.

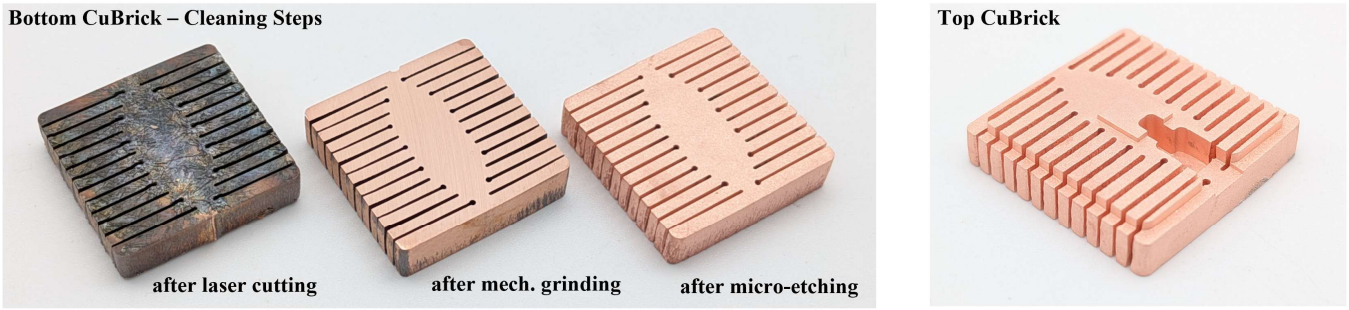


Fig. 7 CuBrick Fabrication a) Bottom CuBrick cleaning steps b) CNC-machined top CuBrick

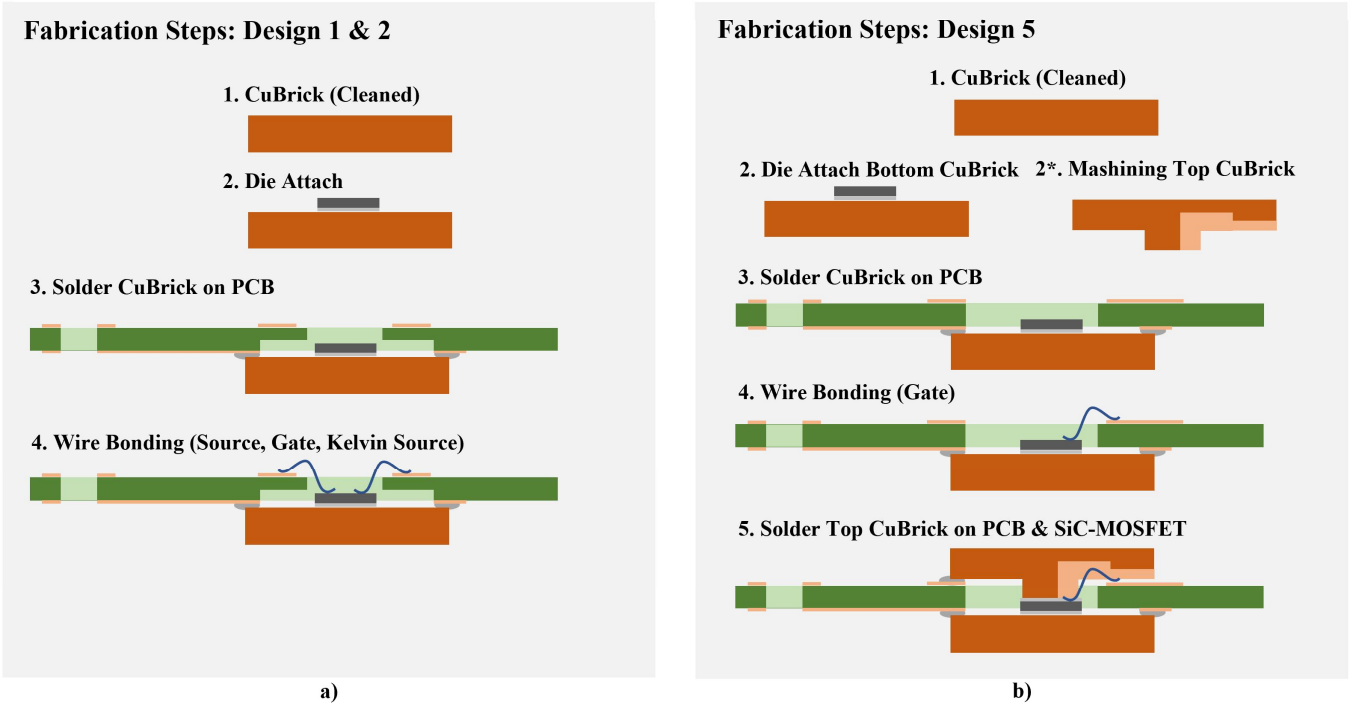


Fig. 8 Fabrication steps for a) single-sided CuBrick configuration (Design 1, 2) b) double-sided CuBrick configuration (Design 5)

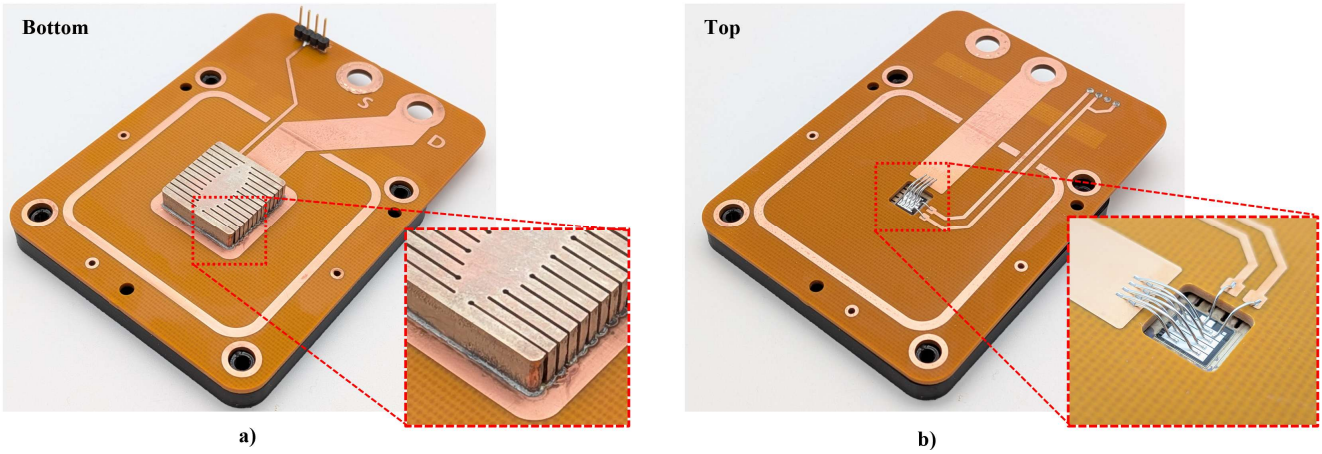


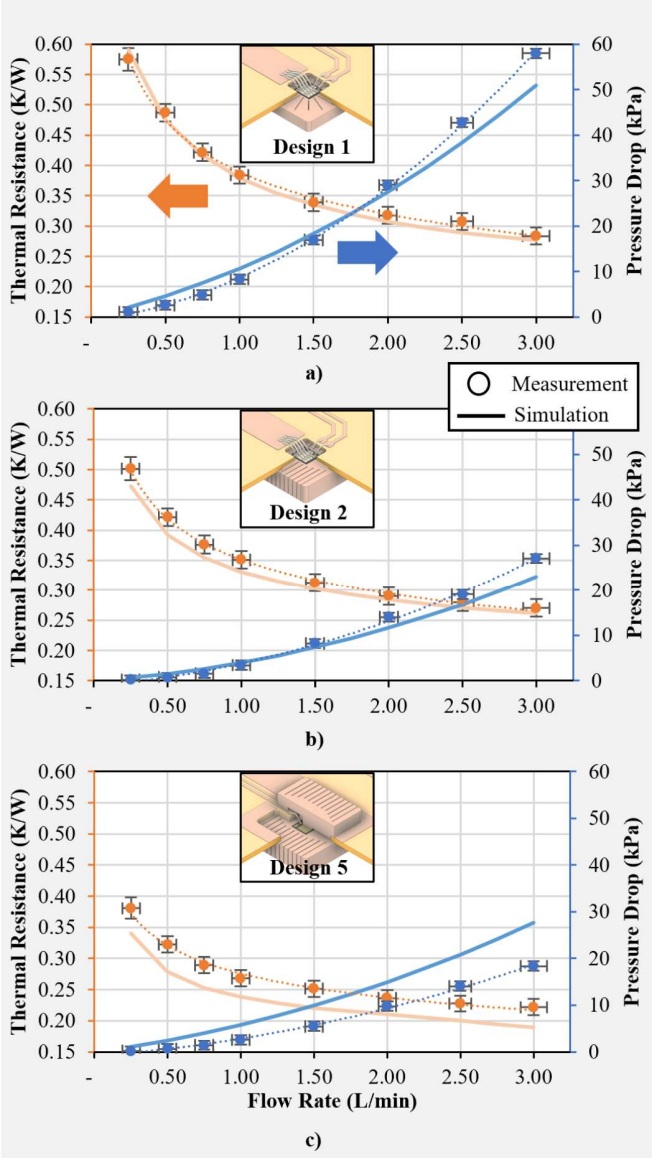
Fig. 9 Fabricated PCB (Design 2) with soldered CuBrick and detail view on a) solder joint b) bond wires

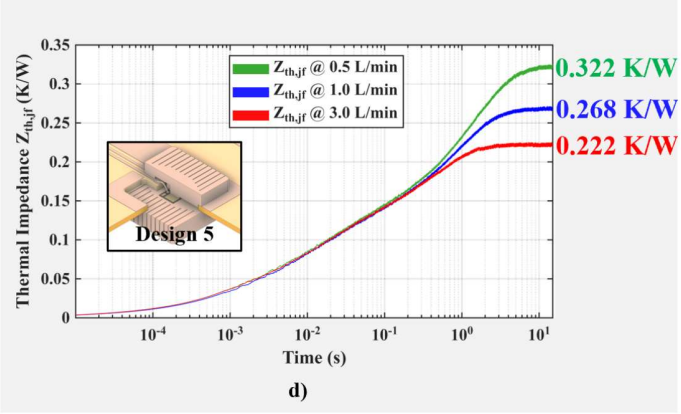
Due to the high thermal mass of the solid copper structures, a double-sided heat input is employed to achieve a reliable solder reflow. The interconnection of the SiC-MOSFET's gate and source pads to the PCB is established using a thick wire bonding process with 300 µm thick aluminium bond wires. This step completes the fabrication workflow for the single-sided configurations (Design 1 & 2). Fig. 9 shows the fully assembled PCB (Design 2) featuring the soldered CuBrick and the chip, which is interconnected via wire bonds.

The double-sided CuBrick variant (Design 5) requires a modified fabrication and assembly flow (see Fig. 8(b). The top CuBrick was fabricated by modifying the bottom CuBrick part via CNC milling, which was used to machine the necessary clearances and cavities (see Fig. 7 (b). To achieve proper alignment between the top CuBrick and the chip, its exact position and orientation was measured using a microscope. The determined deviations were then integrated directly into the CAD-model of the top CuBrick, allowing each component to be individually customized for its respective sample. The top CuBrick, was joined to both the PCB and the chip in a single-step soldering process. For this purpose, solder paste was applied by dispensing onto the PCB and the top-side source metallization. The top CuBrick was then placed onto the PCB and soldered utilizing double-sided heat input.

VI. Results

Fig. 10(a–c) shows the thermal characterization results of the three fabricated prototypes and compares them with the CFD-simulations. For both Design 1 (a) and Design 2 (b), a good correlation between the simulation and experimental data is observable. The error bars correspond to the uncertainty analysis presented in the experimental setup section. Despite the significantly larger heat transfer area provided by the parallel slots and the thicker CuBrick (5 mm), Design 2 exhibits only a small improvement in thermal resistance compared to Design 1 ranging from 0.074 K/W at 0.5 L/min flow rate to 0.014 K/W at 3 L/min. However, the advantage of Design 2 is highly pronounced regarding the pressure drop. Due to the larger number of channels formed by the parallel slots, substantially less





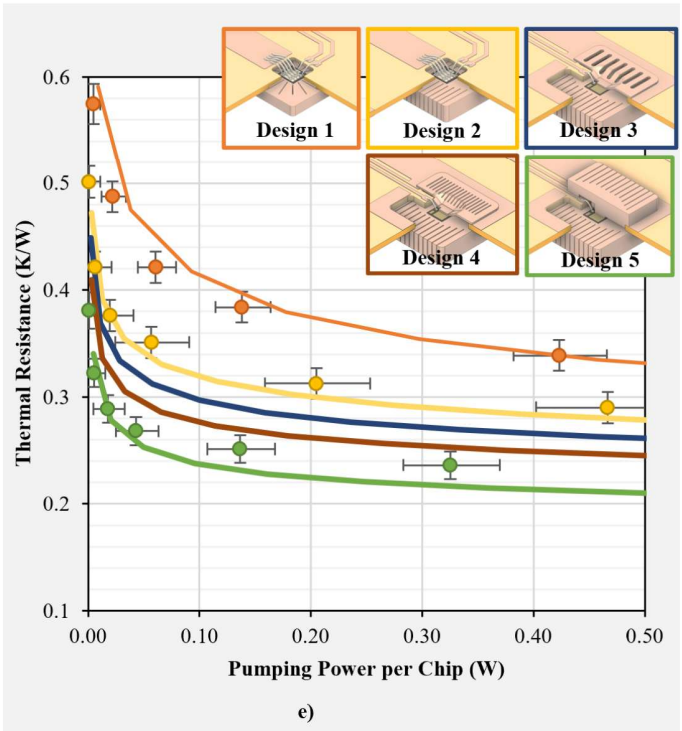


Fig. 10 Results from Measurements and Simulation of a) Design 1 b) Design 2 c) Design 5 d) $Z_{th,jf}$ measurement for Design 5 at three different flow rates e) Comparison of all numerically and experimental investigated CuBrick Designs

hydraulic resistance is generated, resulting in a 50% reduction in pressure drop and, consequently, a halving of the required pumping power.

In contrast, Design 5 (c) shows a distinct discrepancy between the simulation and measurement. Specifically, the measured thermal resistance is approximately 0.04 K/W higher than predicted. This deviation can be attributed to an imperfect thermal interface between the top CuBrick and the chip; since the soldering process was conducted under atmospheric conditions rather than vacuum, the solder layer contains voids that impair heat transfer. The discrepancy in pressure drop could originate from deviations in the slot geometry within the top CuBrick, which remains to be analysed in cross-sectional micrographs. Nonetheless, Design 5 performs best in the experiments, yielding the lowest thermal resistance and the smallest pressure drop. Its thermal advantage stems from the greatly expanded heat transfer area of the top CuBrick, while the hydraulic benefit arises from a simplified flow routing. Whereas the fluid in Designs 1 and 2 converges toward the chip within the recess pocket after penetrating the bottom CuBrick—thereby causing additional hydraulic resistance (see Fig. 1)—the fluid in Design 5 flows straight through both the bottom and top CuBricks.

A representative transient measurement is depicted in Fig. 10(d) by the $Z_{th}(t)$ curve. Here, the transient thermal impedance $Z_{th}(t)$ of Design 5 is plotted for three different flow rates. The curve illustrates the thermal transient response of the chip within the first 15 sec using a logarithmic time scale. Even at a low flow rate of 0.5 L/min, a steady-state thermal resistance R_{th} of 0.322 K/W is achieved. For higher flow rates of 3.0 L/min, an R_{th} as low as 0.222 K/W is feasible.

Fig. 10(e) compares the five investigated CuBrick designs by plotting the thermal resistance as a function of pumping power for both CFD-simulations and experimental measurements. The pumping power is defined as:

$$P_{Pump} = \dot{V} * \Delta p$$

Where $\dot{V}$ is the volumetric flow rate and Δp the pressure drop between inlet and outlet. For Designs 1, 2, and 5, the corresponding experimental data points are included. As previously noted, Design 3 and 4, which utilize TopSheets, were not fabricated or tested; their simulation results serve exclusively for qualitative comparison within the numerical framework. The plot reaffirms the good correlation between measurement and simulation for Designs 1 and 2. This high agreement becomes equally apparent for Design 5 when evaluated against pumping power, as the individual deviations in thermal resistance and pressure drop observed in Fig. 10(c) partially compensate for one another. When analysing the performance curves, a distinct performance offset is visible between Design 1 (radial slots) and the remaining configurations. This is primarily attributed to the high pressure drop of the radial slotted design (see Fig. 10(a)). The implementation of the 5 mm bottom CuBrick with parallel slots (Designs 2–5) provides a substantial advantage here. A further performance enhancement is achieved by integrating top coolers, either in the form of TopSheets (Designs 3, 4) or the top CuBrick (Design 5). With the latter configuration, an R_{th} as low as 0.268 K/W is achieved at a pumping power of 0.043 W and a flow rate of 1 L/min. It should be noted that Designs 1 and 2 utilize different chip sizes compared to Designs 3–5 (see Table I).

VII. Benchmark & Discussion

To evaluate the competitive standing of the CuBrick concept, its thermal performance was benchmarked against a commercial automotive state-of-the-art inverter module (see Fig. 11). The comparison utilizes the chip-area-normalized specific thermal resistance given in mm²K/W and plotted against the required pumping power per chip to ensure a normalized evaluation across different technologies. The primary industrial reference is here the Infineon HybridPack™ Drive (FS05MR12A6MA1B) [11]. This module utilizes four parallelized chips per switch, each with a comparable footprint of 26.7 mm². It achieves a thermal resistance of 0.6 K/W (16 mm²K/W) at a pumping power of only 0.045 W per chip (marked as Ref. and highlighted by a red vertical dashed line in Fig. 11). The reference pin-fin heat sink occupies approximately a 19 x 19 mm area per chip with a 10 mm stack height, nearly identical to the 20 x 20 mm footprint and 10 mm thickness of the double CuBrick

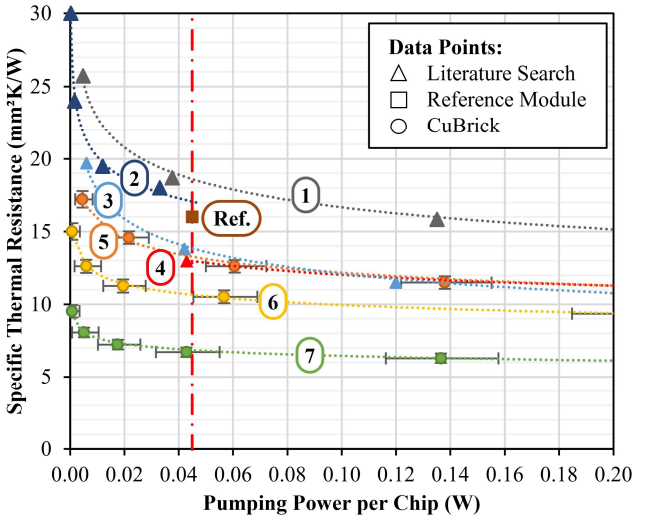


Fig. 11 Benchmark of the CuBrick concept against a reference module and experimental dielectric-cooled set ups from literature

TABLE IV
Literature Search Results For Benchmark (Refers To Fig. 11)

Index:	Reference:	Cooling Approach:	Substrate:	Coolant:
Ref.	[11] Infineon HybridPACK	DBC attached to PinFin cooler	DBC (Si_3N_4)	Water / Glycol
1	[5] Huesgen et al. 2025	Immersion cooling with comibined jet impingenemt and channel flow	PCB	Dielectric
2	[2] Moreno et al. 2022	Chip directly attached to skived Cu heat sink	-	Dielectric
3	[7] Vethake et al. 2025	Micro channel cooler between two isolated DBC-substrates	DBC (AlN)	Dielectric
4	[6] Kamp et al. 2025	Immersion cooling with chip directly attached to pin fin cooler	PCB	Dielectric
	CuBrick:	Immersion Cooling with vertical coolant flow through slotted Cu Blocks	PCB	Dielectric
5	Design 1	One radial slotted 3mm Copper block		
6	Design 2	One parallel slotted 5mm Copper block		
7	Design 5	Two parallel slotted 5mm Copper blocks		

structure (Design 5). This consistency ensures a fair performance comparison within nearly the same volumetric envelope. Furthermore, the comparative analysis is extended by including the state-of-the-art, dielectric-cooled research prototypes introduced earlier. Each dataset is numerically indexed to correspond with Table IV. This table provides a comprehensive overview of the underlying packaging architectures, and specific cooling strategies for each benchmarked system. It can be observed that at the reference pumping power of 0.045 W, the dielectric cooling concepts by Kamp (4) (integrated mini-pin-fin cooler), Vethake (3) (integrated DBC cooler), and the CuBrick Design 1 (radial slots on a 3 mm copper block) exhibit a similar thermal performance of approximately **13.5** mm²K/W. It should be noted that some of these dielectric experimental prototypes utilize a smaller cooling footprint per chip, which influences their position in this benchmark relative to the CuBrick. By simply modifying the slot geometry and increasing the thickness of the copper block—while maintaining the same footprint (Design 2)—the thermal performance of the CuBrick concept can be significantly improved, reaching approximately **10.8** mm²K/W. The benefits of the double-sided cooling concept (Design 5) become particularly evident when comparing the specific thermal resistance. As mentioned earlier, this design incorporates smaller chips (see Table I), reaching a specific thermal resistance of only **6.7** mm²K/W at the reference pumping power. Compared to the 16 mm²K/W provided by the state-of-the-art water/glycol-cooled system, this represents a reduction in specific thermal resistance by a factor of almost **2.4**. This demonstrates that eliminating the ceramic substrate, minimizing the thermal stack, and utilizing double-sided cooling in the CuBrick design more than compensates for the inferior thermophysical properties of dielectric fluids. To the best of the authors knowledge, the specific thermal resistance results presented in this work are the lowest reported for single-phase dielectric cooled power module for SiC-MOSFET with approximately 25 mm² footprint. Consequently, the CuBrick concept establishes a new dielectric cooled performance frontier, outperforming both the established automotive water-cooled pin-fin reference module and the state-of-the-art dielectric-cooled research prototypes.

VIII. Conclussion & Outlook

This paper presented a novel, ceramic-substrate-free dielectric immersion cooling concept for power modules based on modular, perforated copper blocks (‘CuBricks’). By soldering the CuBrick onto a standard PCB and implementing a novel vertical coolant flow directly through the circuit carrier, highly efficient cooling is achieved while maintaining a very simple cooler geometry (e.g. parallel slotted CuBrick).

Within the scope of thermal investigation, two single- and one double-sided design iterations were experimentally characterized using a thermal test vehicle (TTV) and validated via CFD simulations.

The three tested CuBrick variations achieved specific thermal resistances of **13.8**, **10.8** and **6.7** mm²K/W at the reference pumping power per chip of 0.045 W. Notably, all three configurations outperformed the water-glycol-cooled automotive pin-fin reference module, with a specific thermal resistance of 16.0 mm²K/W.

Since the CuBrick concept introduces highly novel approaches to power module packaging, several key challenges remain to be addressed in future research. These include the development of a reliable sealing concept, characterizing the cold-start behavior and degradation (aging) of the dielectric fluid, evaluating material compatibility, and verifying the dielectric strength under high-voltage operating conditions. Consequently, the overall thermo-mechanical and electrical reliability of the module must be systematically investigated. While the distinct thermal advantages of the CuBrick architecture have been successfully demonstrated in this work, future efforts will focus on transitioning the current concept into a functional, full-scale power module, alongside a systematic optimization study of the cooling design.

Acknowledgment

The work presented in this paper was conducted within the Horizon Europe Project “FLAGCHIP” (101172794). The Authors gratefully acknowledge financial support by the European Union. The authors acknowledge the use of Gemini to improve the grammatical flow and phrasing of this manuscript. The authors have reviewed and edited the generated content and take full responsibility for the final version of the paper.

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