FLAGCHIP

FLAGSHIP SOLUTIONS IN POWER ELECTRONICS

D4.7 Public Report of the activities of C&HM

CIRCE

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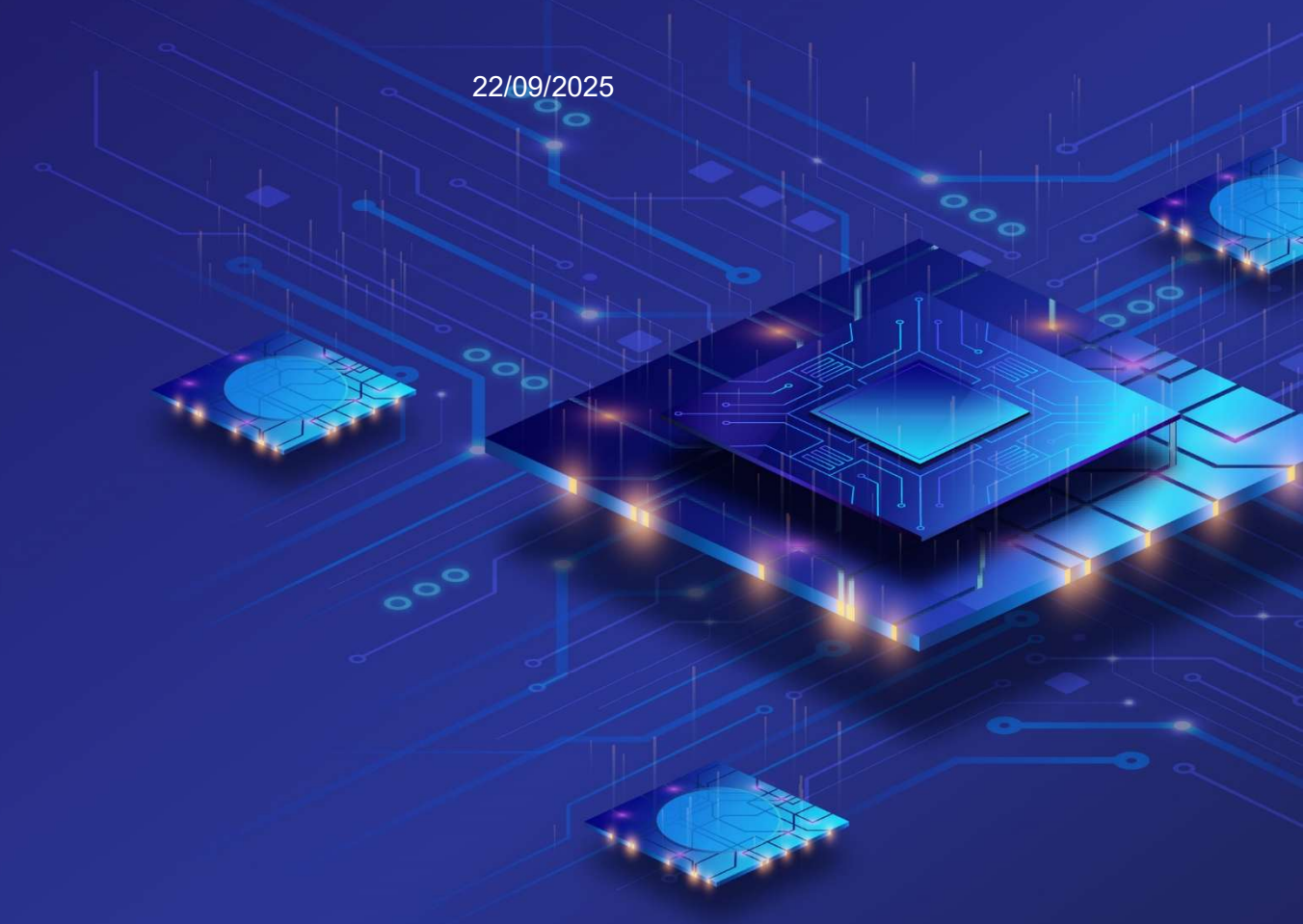

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Executive Summary

This report constitutes the first part of a two-part document focused on the development and validation of Condition and Health Monitoring (C&HM) techniques within FLAGCHIP's Work Package 4. It provides a comprehensive overview of the state-of-the-art in monitoring strategies for power electronic converters, with a particular emphasis on wide-bandgap semiconductor devices such as SiC MOSFETs. The document outlines the foundational methodologies, sensing technologies, and experimental setups used to investigate degradation mechanisms and estimate remaining useful lifetime (RUL). While this report highlights key technical directions and early-stage validations intended for public dissemination, it does not represent the full scope of internal results and proprietary developments carried out within the project.

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List of Terms and Definitions

Table 1. Terms and Definitions

Abbreviation	Definition
C&HM	Condition and Health Monitoring
TSEPs	Thermo-sensitive parameters
MWIR	Mid-wave infrared
EV	Electric Vehicle
FBG	Fibre Bragg Grating
NTC	Negative Temperature Coefficient (thermistor)
IGBT	Insulated-Gate Bipolar Transistor
DDS	Drain-Source Voltage
RDS(on)	On-State Resistance
Vth	Threshold Voltage
Zth	Thermal Impedance
Rgin	Internal Gate Resistance
HMI	Human-Machine Interface
FPGA	Field-Programmable Gate Array
ADC	Analog-to-Digital Converter
PWM	Pulse Width Modulation
DT	Digital Twin

1. Objetives of this document.

This report specifies the non-sensitive information regarding the C&HM developments of the FLAGCHIP project

2. Introduction

Over the last decades, the global push for clean energy — driven by the need for an unlimited, secure and sustainable energy supply — has led to a remarkable decline in the cost of key technologies such as solar panels, wind turbines, battery storage, and electric vehicle (EV) batteries, as shown in Figure 1 from [1] . While the capital cost index for traditional upstream oil and gas has remained stable or even increased slightly, the cost of clean energy equipment has fallen steadily, making renewables and electrified solutions increasingly competitive worldwide. By harnessing inexhaustible resources like solar and wind, countries aim to guarantee long-term energy security and reduce dependence on finite fossil fuels. Crucially, all these technologies — from solar farms to wind turbines, battery storage, and EVs — depend fundamentally on power electronics (PE) to operate efficiently and reliably. Inverters, converters, and advanced semiconductor devices manage the flow and conversion of electricity at every stage, making it possible to harness, store, and deliver clean energy when it is needed.

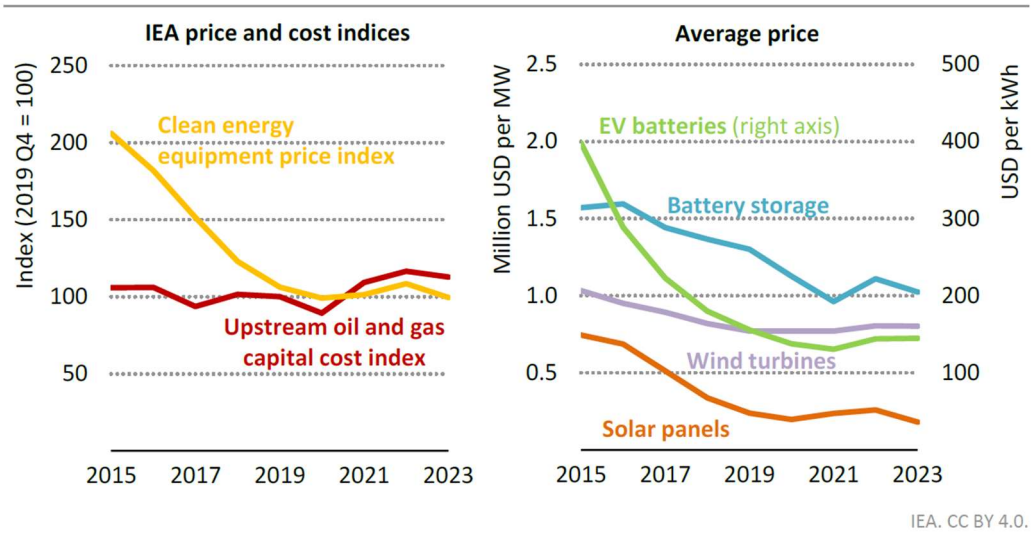

Figure 1: IEA indices for clean energy and upstream oil and gas, and global average price of selected clean energy technologies [1].

However, increased deployment of PE also increases the importance of reliability. Power electronic systems are often expected to operate continuously in critical roles – e.g. in an electric vehicle's drivetrain or a wind turbine's converter – where any downtime can be costly or disruptive. Therefore, the reliability of these systems is critical, as failures can result in significant economic losses, safety hazards and environmental impacts. Ensuring that power converters remain operational over long service lifetimes underpins the viability of technologies ranging from fast-charging EV stations to smart

grids. A notable challenge with power electronics is that they often fail silently and without obvious external warning signs, unlike many mechanical systems. Mechanical equipment (like engines or gearboxes) may exhibit audible noise, vibration, or visible wear as they degrade, providing cues for maintenance. In contrast, power electronics components can degrade internally with little to no obvious indication until a sudden failure occurs.

One of the main reliability challenges in power electronic systems is related to the vulnerability of critical components, especially capacitors and power transistors. Transistors are particularly susceptible to thermal stress due to internal power losses, leading to repeated cycles of heating and cooling—known as thermal cycling or power cycling. These thermal cycles cause thermomechanical stresses resulting from mismatches in thermal expansion coefficients among transistor components, such as wire bonds and solder layers, accelerating their degradation and ultimately leading to premature failures [2]. This degradation is particularly critical in applications where power electronics play an essential role in system safety and continuity, such as electric vehicles, wind turbines, photovoltaic systems, and aerospace. Consequently, the deployment of advanced Condition and Health Monitoring (C&HM) techniques gains special importance, as these approaches enable early detection of silent failures, optimize maintenance strategies, prevent costly downtimes, and extend transistor lifetime.

Figure 2 condenses two decades of research into a single left-to-right timeline, showing how condition-monitoring (CM) techniques for power-device reliability have progressed from invasive, laboratory-only measurements to fast, in-situ diagnostics. At the left-hand edge (≈ 2000) we find *physical contact* approaches—thermocouples, liquid-crystal coatings, etc.—that required dismantling the package. Around 2005, engineers began exploiting electrical thermo-sensitive parameters (TSEPs) such as the on-state voltage at low current and the saturation current, which could be probed through the device terminals with minimal interruption to operation. The next milestone (≈ 2010) was the use of the gate-threshold voltage and the NTC/diode test chips embedded in commercial modules, followed quickly by gate turn-off voltage sensing—methods that enabled on-line temperature estimation with good linearity.

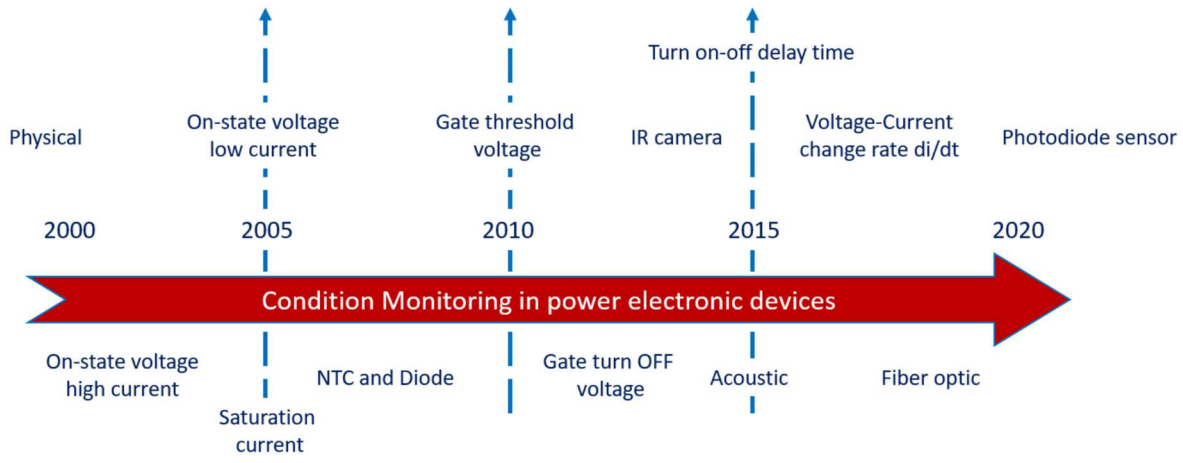

Figure 2: Overview of key condition monitoring (CM) methods implemented during the last twenty years [3].

By 2015 the focus had shifted towards *dynamic* signatures: turn-on/turn-off delay times, dV/dt and dI/dt, captured with high-bandwidth probes, while infra-red cameras and the first acoustic emission studies added contact-less options for laboratory validation. The most recent additions (post-2018) exploit fiber-optic sensors and the internal photodiode/electroluminescence of SiC devices, allowing completely galvanic-isolated, sub-microsecond junction-temperature tracking inside high-voltage modules.

Although condition- and health-monitoring (C&HM) techniques have matured enormously, their integration into a commercial power converter is never free of trade-offs. In many low- to medium-power products the additional bill-of-materials for temperature-sensing diodes, fiber-optic probes or high-bandwidth measurement electronics can eclipse the expected savings from longer lifetime. Even “sensor-less” approaches—those that infer junction temperature from on-state voltage or switching transients—still call for Kelvin-sense terminals, precision amplifiers and extra gate-drive circuitry that are absent from strictly cost-optimized designs. Beyond cost, the very act of adding hardware can create new reliability concerns: every extra wire-bond, solder joint or lid feed-through introduces another mismatch in thermal expansion, another hotspot for fatigue, and in some cases a parasitic inductance that worsens voltage overshoot during fast SiC or GaN switching.

A second layer of difficulty appears once the system is in the field. Sensors drift, opto-windows cloud, wire-bonds age: unless the monitoring chain is recalibrated, its readings lose accuracy and may trigger false alarms or, worse, mask genuine faults. Techniques that rely on low-current voltage probes or saturation-current pulses often require brief load interruptions; in round-the-clock service that interruption itself can be unacceptable. Meanwhile, high-speed waveform capture produces torrents of data that must be filtered, stored and interpreted—tasks that add software complexity and can overwhelm operators if the diagnostic thresholds are not finely tuned.

Yet there are clear applications where C&HM justifies its own overhead. In multi-megawatt wind turbines, HVDC converters, ship drives or 800-V fast-charging stations, a single unplanned outage can cost far more than a suite of embedded sensors; here, real-time junction-temperature insight empowers predictive maintenance and derating strategies that avert catastrophic shutdowns. Likewise, aerospace power units, medical imaging supplies and other mission-critical platforms demand the early-warning capability that C&HM provides, because component failure translates directly into safety risk. Finally, in capital-intensive, high-density SiC or GaN modules—where each package already represents a sizeable investment—the incremental footprint and cost of monitoring hardware are small compared with the gains in service life, warranty confidence and data-driven design feedback.

The preceding sections have shown that deploying Condition & Health Monitoring in power converters is no longer a purely academic exercise: it is a technical necessity wherever high-value assets, wide-band-gap devices and demanding duty cycles converge. At the same time, we have identified the practical barriers that still hinder large-scale adoption—chief among them measurement cost, sensor intrusiveness and the need for robust lifetime models that translate raw data into maintenance decisions. With these challenges in mind, Work Package 4 (WP4) of the FLAGCHIP project will move beyond state-of-the-art surveys and deliver a concrete, multi-layer framework that couples accurate junction-temperature sensing with degradation tracking and lifetime-aware control.

There has been done a benchmarking four complementary temperature-estimation techniques for SiC MOSFETs—internal-gate-resistance sensing, GaAs band-gap transducers, on-state Vds probing and Fiber-Bragg-Grating (FBG) optics (Task 4.1). This comparative study will quantify the accuracy-versus-cost trade-off highlighted earlier and will generate prototype hardware that partners can integrate into renewable-energy test benches. Building on those measurements, Task 4.2 it will monitor the health of the power-module stack at three different hierarchy levels—chip, bond-wire and substrate—so that electrical, thermal and mechanical degradation paths can be distinguished in real time. The resulting data streams will be distilled into actionable degradation markers capable of triggering a limp-mode strategy that derates the converter once a critical tipping point between instantaneous power and remaining useful lifetime is reached.

To close the loop between monitoring and operation, it will implement a lightweight extrapolation method that predicts remaining useful lifetime (RUL) from incremental changes in key parameters, avoiding the calibration overhead that currently limits field use. The RUL estimator will feed both a real-time digital-twin board (Task 4.5) and advanced control-strategy simulations (Task 4.6), enabling on-board detection of parameter drift and system-level optimization under resonant, variable-DC-link scenarios. Taken together, these tightly inter-linked tasks will convert the conceptual advances discussed in this introduction into validated hardware, firmware and modelling tools—demonstrating that cost-effective, minimally intrusive C&HM is not only feasible but also instrumental for extending the life and reliability of next-generation power-electronic converters.

3. Understanding and Anticipating Failures in SiC Power Modules Through Accelerated Aging and Monitoring

3.1 Anticipating a Failure: A Major Challenge

Conditioning and Health Monitoring (CHM) techniques remain a complex field, with significant difficulty in identifying degradations. The purpose of CHM is to anticipate a failure and adjust the module's performance in case preventive maintenance is needed, thereby ensuring service continuity.

The main challenge is to correctly identify degradations early enough, which is not straightforward for technologies such as SiC that are less well understood or behave differently compared to silicon, which has been used for decades. In fact, degradations are particularly difficult to assess since they often occur without any known precursor signs [4][6]. Identifying a potential malfunction therefore consists of finding reliable indicators of aging.

Estimating the lifetime of components also requires precise knowledge of the junction temperature, which remains difficult to achieve today. Direct measurement is impossible, as it would be far too invasive in the area considered the most critical, and achieving sufficient accuracy appears complex [7]-[9]. Nevertheless, it can be estimated using different techniques.

Real-time measurement of electrical parameters is one possibility. Since the module's electrical parameters evolve with temperature, these quantities—called TSEPs (Temperature-Sensitive Electrical Parameters)—can be used to estimate the junction temperature [9]-[11]. Among these parameters are the drain-source voltage V_{DS}, the on-state resistance $R_{DS(ON)}$, the threshold voltage Vth, the thermal impedance Z_{th} and the internal gate resistance (R_{gin}). The major difficulty lies in the fact that these TSEPs are also sensitive to degradations in the module and will therefore vary as it ages. Their drift over time, due to degradation, may then lead to a distorted real-time estimation of temperature. They are then referred to as DSEPs (Degradation-Sensitive Electrical Parameters). The challenge is thus to determine whether the observed variation is caused by a temperature rise or by degradation of the power module [10].

3.2 Understanding Degradation Mechanisms

Understanding Degradation Mechanisms

It is therefore essential to have a precise understanding of degradation mechanisms and their effects in order to distinguish whether the observed parametric variations are caused by a temperature rise or by degradations experienced by the module.

Overall, the main families of degradation are similar to those found in IGBT modules, but with specific features that make the task more complex than it may seem. Indeed, for voltage levels still considered reasonable with respect to the maturity of SiC (<3.3 kV), SiC MOSFETs stand out thanks to their higher power density, operating temperature range, and switching frequency compared to their silicon counterparts. Specific degradation mechanisms linked to SiC may therefore emerge [4],[5],[11].

Different regions and mechanisms of degradation can thus be identified.

[11] summarizes in the figure below the different types of degradation that can be encountered in SiC chips.

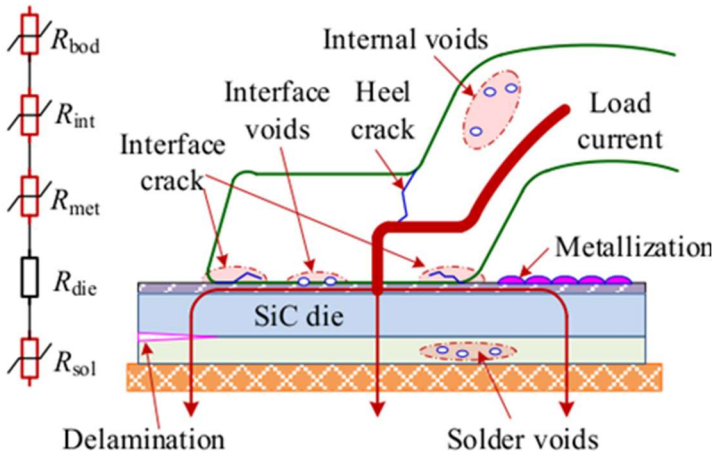

Figure 3 : Package Degradation Mechanisms from [8

Degradations can thus be found at different levels of the package. They may appear in the bonding wires [6],[12] as well as at their interfaces with the chip [11],[14], or within the metallization, particularly at the chip–substrate interconnection [4],[14],[15]. Degradations within the chip itself must also be taken into account [4],[5],[7] .

3.3 Power Cycling: A Tool for Analysis and Accelerated Degradation

Understanding the degradation of SiC power modules remains a complex matter. These modules are intended to operate for several decades, and it is not feasible to wait that long to study each degradation mechanism.

The objective here is to accelerate the aging of SiC MOSFET power modules through relatively rapid heating–cooling cycles. The aim is to raise the MOSFET junction temperature to levels approaching 150 °C as shown in figure 3. This accelerated aging is achieved by driving high current (250 A) and switching the MOSFETs at frequencies up to 10 kHz. Unlike DC cycling, which only involves conduction, AC cycling includes switching events and thus more closely replicates real operating conditions.

This repeated alternation of heating and cooling cycles therefore makes it possible to accelerate aging and to observe potential degradations of the module within a few weeks or months, whereas in real operation this would take several decades.

The aging is carried out using an H-bridge structure with an inductive load, as shown in Figure 4 Electrical Scheme of the Power-Cycling Test-Bench. The test bench alternates between charging and

discharging phases of the inductance depending on the MOSFET switching state. The inductance is recharged by appropriately sized capacitors, while a back-to-back supply configuration is used so that only the losses are provided.

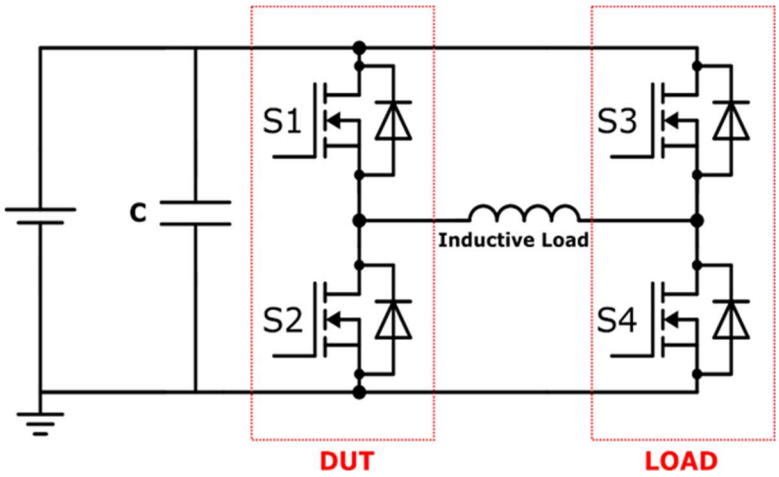

Figure 4 Electrical Scheme of the Power-Cycling Test-Bench

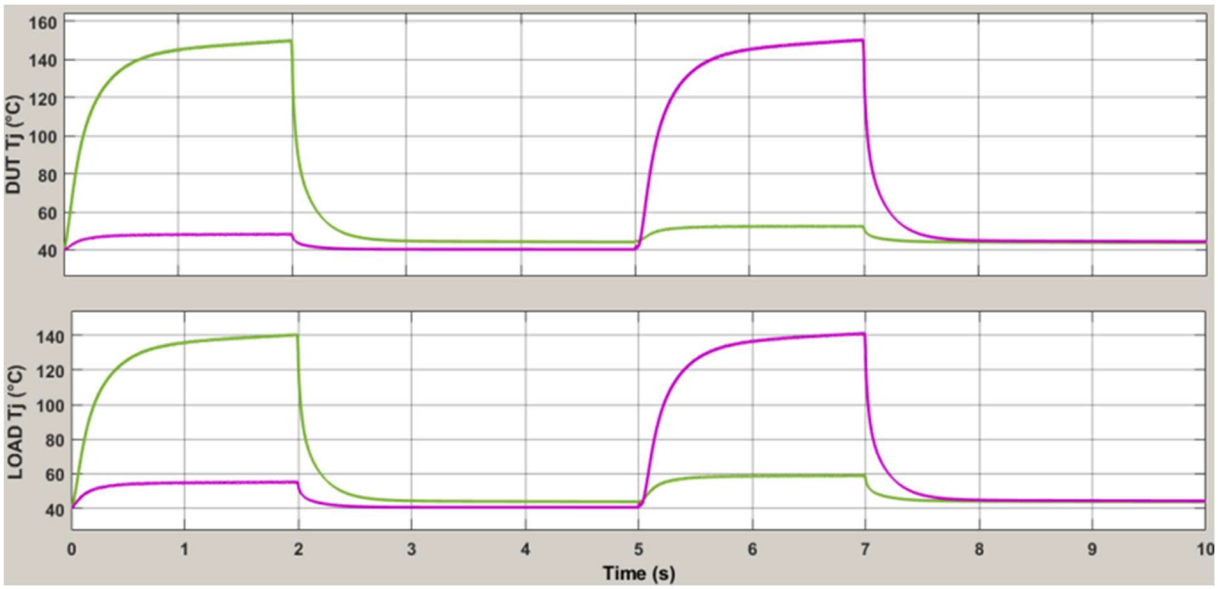

Figure 5: Evolution of the (simulated) junction temperature for DUT and LOAD modules (green: High-side, purple: Low-side)

This aging procedure serves several purposes. First, under test conditions up to component failure, the power cycling bench makes it possible to estimate the number of cycles a module can withstand, and thus its lifetime. Lifetime estimation can be derived using Miner's rule [16],[17], which assumes that the total lifetime can be calculated by summing the fractions of lifetime consumed by each stress cycle.

$$D = \sum_{i=1}^{km} \frac{n_i}{N_{f,i}}$$

Equation 1: Total Lifetime considering each stress cycle

With n_i : the total number of cycles in the i-th block of a constant stress amplitude

K_n : the total number of stress blocks

$N_{f,I}$: the number of cycles to fail under a constant stress amplitude

Based on the Palmgren-Miner linear damage hypothesis, failure is expected to occur when the damage accumulation factor D > 1

Combined with different test criteria, known as Mission Profiles, the Remaining Useful Lifetime (RUL) can be estimated. This information is particularly valuable for end users, as it enables planning for module replacement or reducing the device load until the next maintenance. In this way, prolonged downtime can be avoided.

The degradation analysis described above relies on measuring various parameters, including junction temperature, VDS, RDS(on), Vth, and Zth.

One of the main difficulties was the need to repeatedly disassemble and reassemble the modules for characterization with a B1505 curve tracer. Since reassembly on the test bench was never perfectly identical to the previous mounting, this procedure inevitably introduced significant measurement uncertainties. To address this, dedicated in-situ measurement boards were developed, enabling all measurements to be performed directly on the test bench without module removal. This approach improves measurement reliability. The junction temperature measurement board provided by MERCE will be integrated into this set of boards, thus offering a complete and reliable monitoring solution.

4. On-Chip Temperature Monitoring During Power Cycling via Fibre Bragg Grating-Based Sensors

4.1 Overview

FBG sensors provide an electrically isolated temperature measurement, which can be utilized for fast and accurate semiconductor junction temperature (T_j) estimation. Assessment of the thermomechanical stresses from power cycling of the power semiconductor, and evaluation of RUL as part of C&HM requires such a temperature measurement.

Common to the packaging of some high-voltage power module platforms is the inclusion of negative temperature coefficient (NTC) thermistors, which allow for temperature monitoring at the package substrate. The drawback of this approach is that the thermistors are located far from the devices and consequently lead to poor inference of T_j.

Another widely adopted approach for T_j measurement is the use of semiconductor TSEPs, offering far greater accuracy than the use of embedded NTC thermistors. Measurable at the device terminals, TSEPs are specific to device technology [18], package layout, and can vary with device ageing [19]. Consequently, a significant amount of work is involved in the calibration of dedicated TSEPs, which are not universally applicable to power electronics devices and challenge their applications for real-time on-line monitoring.

Recently, FBG temperature measurement approaches have been applied in the baseplate underneath power semiconductor devices [20], demonstrating the capability of a single fibre for distributed temperature measurement. This was later applied to IGBT press-pack modules, where the sensors were integrated into molybdenum platelets for in situ chip temperature measurement [21]. Other researchers investigated the applicability of the FBG technology for on-chip temperature measurement in insulated gate bipolar transistor (IGBT) power modules [22]-[24]. The positioning and interfacing of the sensing head were studied, finding that a high quality, yet yielding, thermal interface positioned at the hot spot of the device improved measurement accuracy and transient response.

The contribution of UoN to this work package has been to provide a detailed analysis of calibration, implementation and measurement error of temperature measurement using FBG sensors. The study has focused on a power cycling test bench of representative samples, building a foundation for the integration of FBGs into full power electronics modules (PEMs) in the future.

4.2 Fibre Bragg grating sensor theory

A functional FBG sensor is created by a periodic inscription of the core of an optical fibre, serving to adjust its refractive index at those points. The fibre reflects light of the central Bragg wavelength, λ_B, related to the period of the grating, Λ, by (1), and transmits other light [23],[25].

$$\lambda_B = 2 \cdot \Lambda \cdot n_{eff} \quad (1)$$

where n_{eff} is the effective refractive index of the fibre.

Variation of the temperature, ΔT, or strain, $\Delta\varepsilon$, acting upon the fibre causes a commensurate variation in the reflected wavelength, $\Delta\lambda_B$, given by (2).

$$\Delta\lambda_B/\lambda_B = \Delta T(\alpha + \xi) + \Delta\varepsilon(1 - p_{eff}) \quad (2)$$

where α is the thermal expansion coefficient of the fibre, ξ is the thermo-optic coefficient of the fibre, and p_{eff} is the photo-elastic constant for the fibre.

In a constant strain or strain-free configuration for the sensing head, the reflected wavelength is sensitive only to variation in temperature, as represented by (3) [23].

$$\Delta\lambda_B = \lambda_B \cdot \Delta T \cdot (\alpha + \xi) \quad (3)$$

Such sensors have reported a calibrated sensitivity for similar sensors of 10–14 $\mathrm{pm} \cdot {}^{\circ}\mathrm{C}^{-1}$. Key features for a typical FBG are shown in Figure 3.

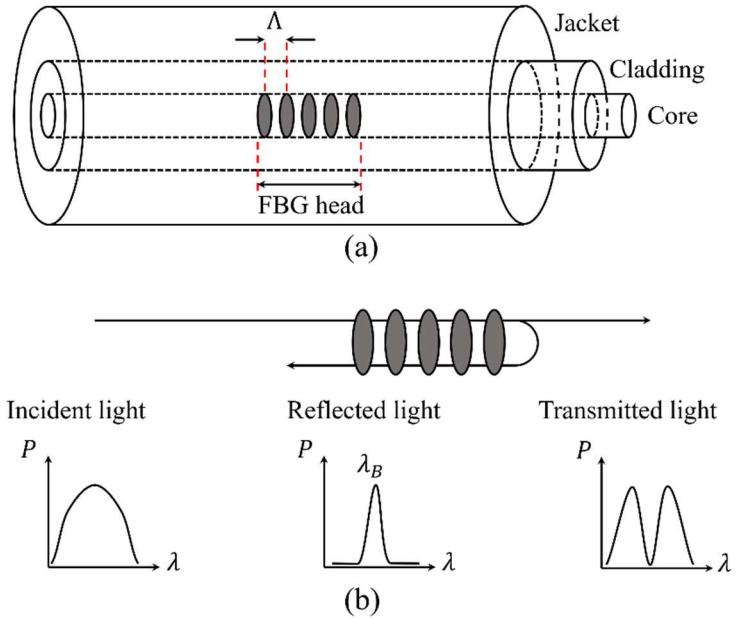

Figure 6: FBG characteristics: (a) structure, (b) light propagation.

4.3 Calibration of FBG sensors

Determination the wavelength-to-temperature relationship of a FBG sensor is possible through heating the fibre to increasing temperatures, and pausing until steady-state is achieved at each stage whereupon the current wavelength is recorded. The $\lambda - T$ mapping is then performed using an appropriate model.

For calibration of FBG sensors in this work, samples were subjected to periodically increasing temperatures in the range 40–160 °C. The fibre was fastened at one end only to ensure no strain was induced at the point of the sensing head. Figure 7 shows fitting results for linear and quadratic models given, following the approach of other authors [20],[22].

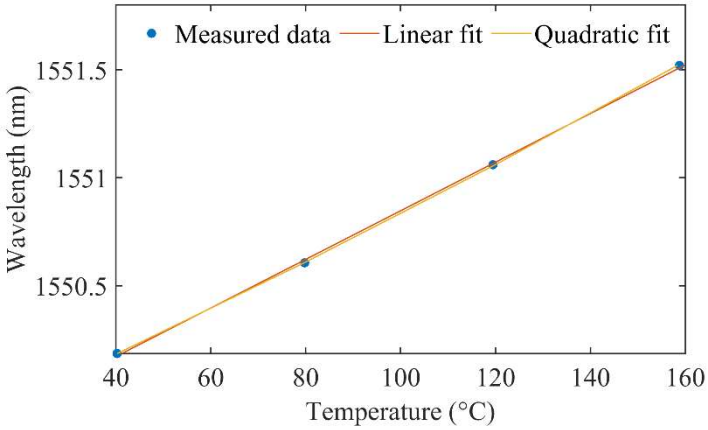

Figure 7: Calibration results for FBG sensor with linear and quadratic models.

4.4 Temperature measurement under power cycling

Due to their construction, semiconductor dies are not always uniformly heated during power cycling, which can make optimal placement of FBG sensors difficult. To demonstrate how this can be overcome, a mid-wave infrared (MWIR) imaging camera was used to record the thermal contours of the samples under power cycling. For the diode dies in this work, the locus of heat generation was in the centre of the die, corresponding with the centre of the active area of the chip, which was the position chosen for the FBG sensing head. Figure 8 shows a photograph of a diode test vehicle with FBG sensor attached.

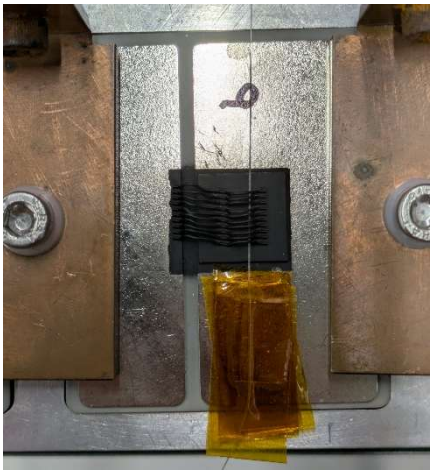

Figure 8: Photograph of diode test vehicle with FBG sensor attached, in situ of power cycling equipment

Significant transient temperature measurement error was observed during initial testing at 40 A between 40–90 °C. A single cycle is shown in Figure 9. This error is attributed to a thermal network consisting of the layers of acrylate material surrounding the FBG core and the potential of a slight air-gap between the fibre and the diode surface. Additional trials with varying heating currents 35–60 A were performed to further evaluate the transient response. Higher heating currents, and

commensurately reduced heating times, showed an increase in the temperature measurement error. The greatest error was always shown to be during the heating transient.

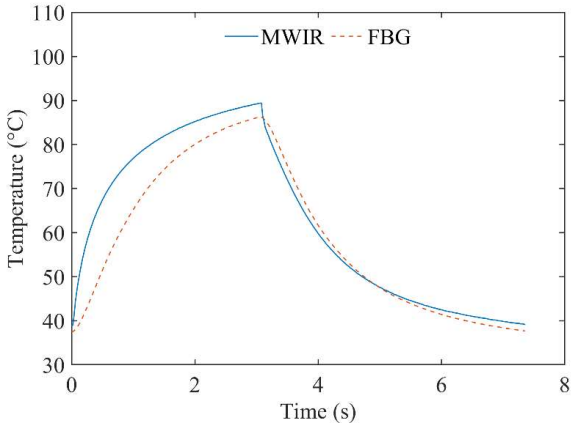

Figure 9: Comparison of measured chip temperature (MWIR) and interpreted FBG temperature measurement (FBG) under power cycling at 40 A.

4.5 Transient response improvements

Clearly, the observed temperature measurement error makes the configuration incompatible with the aim of fast and accurate T_j estimation, and error mitigation must be sought. As discussed in [26], the material surrounding the FBG has a significant influence on the transient response. This is also investigated in [24], where an air-gap between the FBG and die resulted in larger error compared to a solid thermal interface. This was developed further in [22], with an investigation into adhesives for FBG-die bonding.

Subject to appropriate calibration methods, these works found that an additional thermal interface improved the transient response and provided no additional strain-induced error. However, integration of an adhesive thermal interface into module packaging could be difficult, and the long-term viability of the interface is not yet studied.

As a result, an effort was undertaken to better understand the influence of an air-gap on the FBG transient response and evaluate the potential for easy mitigation through removal of the fibre jacket.

Finite element transient thermal simulations carried out in ANSYS Fluent 2D showed that even at only 200 µm above the die surface, the temperature was reduced by over 2 °C. Considering the challenges involved in co-packaging these sensors, a gap in excess of this value could easily be created in practice. Simulations including the FBG with and without the jacket with a fixed air-gap of 50 µm were then carried out, with results shown in Figure 9, wherein the bare fibre is shown to improve the transient response.

Experimental validation was then sought for the simulation result. The fibre jacket was easily removed using appropriate tools, and the power cycling trials were repeated (40 A, 40–90 °C). A single cycle from these trials is shown in Figure 11, clearly demonstrating the reduction in temperature measurement error, and highlighting jacket removal as a candidate for continued work.

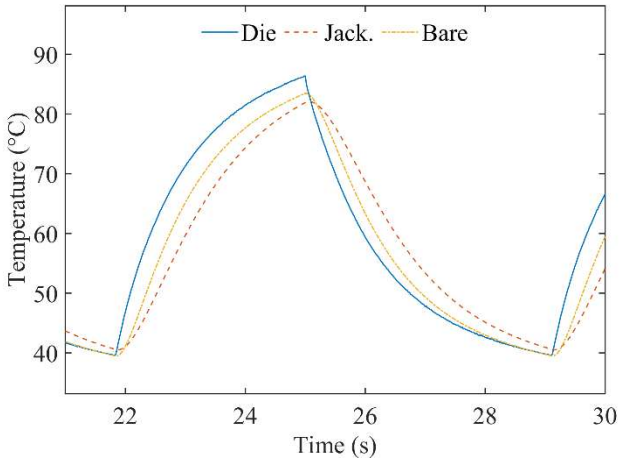

Figure 10: Simulated thermal profiles of the die (blue, solid), FBG core with jacket (orange, dashed) and FBG core without jacket (yellow, dash-dot) under power cycling.

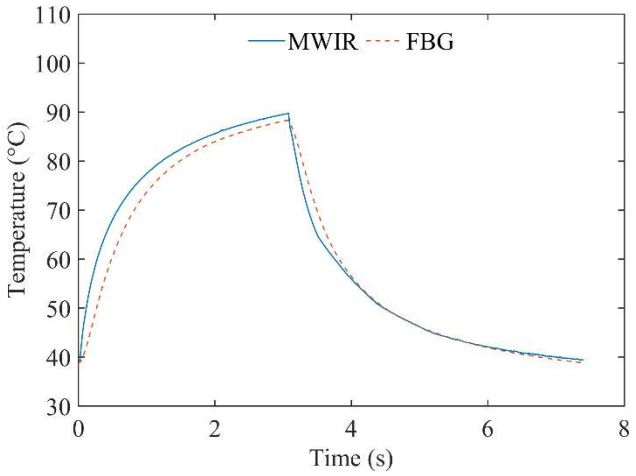

Figure 11: Comparison of measured chip temperature (MWIR) and interpreted FBG temperature measurement (FBG) under power cycling at 40 A, using jacketless sensor.

4.6 Outlook

Though the FBG with jacket removed achieved a better transient response, investigations into the suitability of this approach are required, especially considering the fragility of the jacketless fibre.

Using the established literature as a springboard, evaluations of the thermal adhesive are also to be carried out. Though the operating temperatures of a typical power device are within the manufacturer limits for the best candidate thermal interface material, an understanding of its long-term degradation under temperature cycling is required.

Similarly, a C&HM solution designed to evaluate RUL of a device or module needs itself to degrade little over the expected lifetime, and so thermal-shock trials are being carried out on the fibres themselves, in isolation.

Finally, it is possible to inscribe multiple FBG sensors into a single fibre, offering potentially reduced packaging complexity. Investigations into best practices for multi-chip single-fibre and single-chip multi-point single-fibre configurations are currently underway.

5. Junction Temperature estimation using the internal gate resistance as TSEP

Using a Temperature Sensitive Electrical Parameter (TSEP) to measure the junction temperature represents a high interest to estimate online the junction temperature. This allows to get access of the junction temperature without additional sensor and therefore reduce the cost. Several challenges must be overcome to use this method. First, the calibration is a necessary step to obtain the variation of the electrical parameters of the TSEP with the temperature. This process of calibration can vary in complexity depending on the type of TSEP. Moreover, the parameters of each transistor remain unique depending on the manufacturing process which involves that the calibration must be performed for each device. Secondly, the implementation of the temperature estimation in an industrial application requires the ability to monitor the temperature irrespective to the operation conditions. This implies that the TSEP method must be not influenced by the power conditions such as the bus voltage, the load current and the switching. Moreover, an online method must have a limited intrusively to not disturb and influence the nominal operation of the system. Finally, the TSEP methods must be robust during the aging of the devices with a limited deviation during the lifetime of the device.

The method based on the internal gate resistor, $R_{gin}(T_j)$ shows good immunity with the load conditions. Moreover, this technic doesn't require specific power connection and the connections present on all power modules are sufficient to use this technic. The only limitation may come from the design of the power module where the implementation of the gate resistance must be present on the chip to be able to measure the junction temperature of the dies in the power module. The results obtained on IGBT technology show robust results with a good precision of ± 2°C and good accuracy independent on the operation condition (Load current and Bus voltage) [27].

The main principle to measure the internal gate resistance during the power converter operation, is based on the injection of a DC current (Ig) through the gate source path during a controlled time duration, as shown in Figure 12.

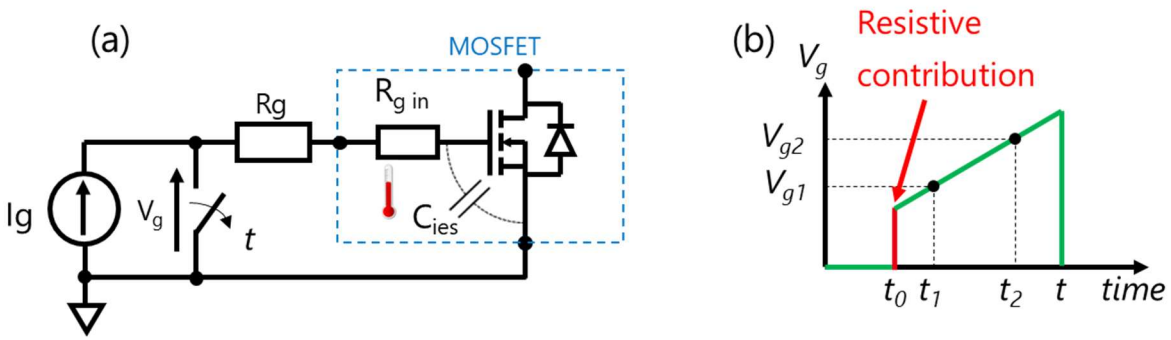

Figure 12: Schematics of the current injection on the gate (a) and the theoretical waveform (b).

The current injection is controlled by a bypass switch that shorts the current source when the switch is ON. By turning OFF the switch during a control time, the current is injected through the gate. The voltage can be described by the following equation (1):

$$V_g = R_{gin}(T_j) \times I_g + \frac{t}{C_{iss}} \times I_g \quad (1)$$

The voltage response across the device at t0 is related to the resistance R_{gin}, followed by a slope corresponding to the charging or discharging of the gate capacitor C_{iss}. $R_{gin}(T_j)$ is linearly depends on the temperature according to equation (2):

$$R_{gin}(T_j) = (\delta R_g \cdot T_j + 1) R_{g0} \quad (2)$$

Where R_{g0} is the internal gate resistance at 0°C and δR_g is the relative variation of the resistance with temperature. The junction temperature is measured online, in a non-intrusive context on a MOSFET controlled with a voltage-source gate driver. The junction temperature measurement functionality can be made during the nominal operation of the MOSFET by controlling the injection within the PWM, as shown in Figure 13. Note that the figure is not in scale, where the injection is duration is in the range below 1µs and a voltage amplitude below 1V to avoid any perturbation of the nominal operation of the MOSFET.

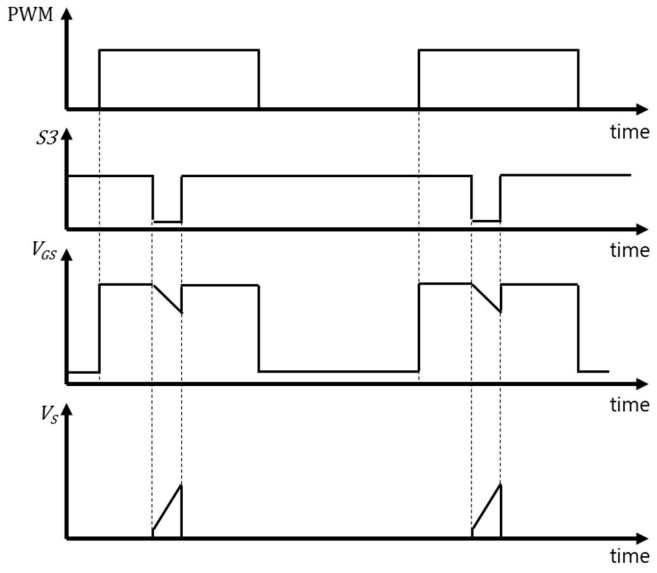

Figure 13: The signals of temperature measurement sequence synchronised on the MOSFET operation.

The different signals of the temperature measurement are synchronised on the MOSFET operation PWM. The gate voltage Vgs is set by the gate driver voltage source which changes from a negative to a positive value. Choosing the initial voltage to start the junction temperature is necessary to operate the Tj estimator properly. The Tj measurement sequence is controlled by a CPU or FPGA which synchronises the current injection timing with the PWM signal to start the injection in steady state avoiding gate voltage switching perturbation. The FPGA control the timing ADC measurement precisely to get the voltage measurement at the good instance. The timing synchronisation is highly important to increase the precision and for instance jitters on the process may affect the measurement.

As results, the Figure 14 shows an example of calibration of the TSEP which allows to determine the variation between the TSEP and the junction temperature.

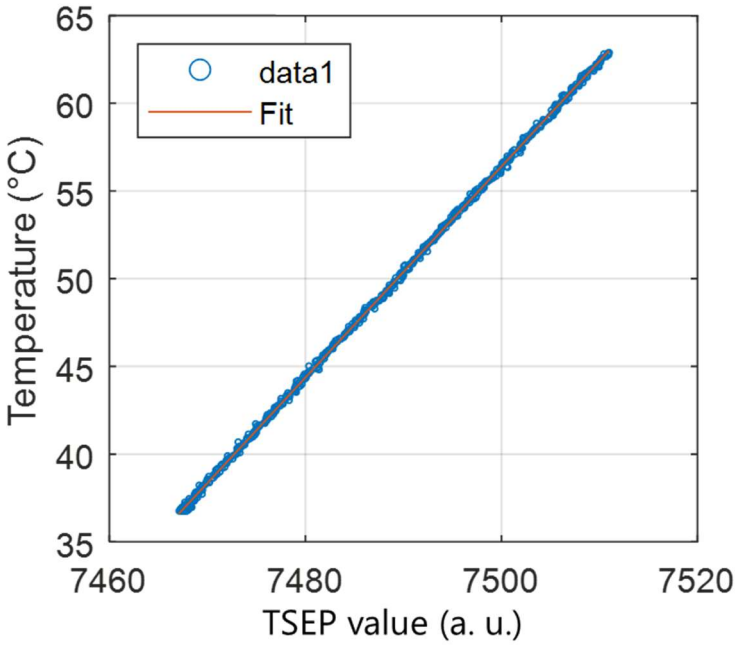

Figure 14: Example of calibration results obtained for a SiC MOSFET.

6. Digital-Twin Architecture for Power-Converter Condition & Health Monitoring

Another promising approach for Condition and Health Monitoring (C&HM) not only detects device degradation but also proactively predicts and manages it through innovative methodologies such as the digital twin. Digital-twin technology offers a path around these compromises by creating a physics- or data-driven software replica of the transistor and its thermal environment that runs in lock-step with the real hardware**.** The twin ingests the same gate commands, dc-link voltage and phase currents that the device experiences, then predicts junction temperature, conduction losses and even incipient parameter drift without extra physical instrumentation. Because the model is constantly updated with live measurements, it can spot a divergence—say, a rising VDS(on) or an anomalous switching waveform—long before conventional protection trips.

The strength of digital-twin-based monitoring lies in its capability to provide deep insight into the internal state of the device without necessitating intrusive physical instrumentation. By continuously correlating real-world data with high-fidelity models, the digital twin enables early identification of subtle, yet critical, shifts in device parameters such as threshold voltage, internal gate resistance, and thermal impedance. This real-time visibility not only enhances the reliability of power electronic systems but also facilitates predictive maintenance, allowing interventions to be scheduled before minor degradations evolve into major failures.

Moreover, the digital twin supports proactive lifetime management strategies by simulating future operating conditions based on historical and current performance data. Through virtual scenario testing—varying loads, switching frequencies, or environmental conditions—the digital twin can anticipate potential stress points and recommend operational adjustments or de-rating actions. This capability ensures the converter maintains optimal performance while significantly extending the transistor’s lifetime, thereby maximizing asset utilization and reducing overall operational costs.

Finally, implementing digital-twin technology aligns naturally with modern developments in power electronics, such as wide-bandgap semiconductor devices and compact, high-power-density converters. The digital twin complements these advancements by providing real-time diagnostic feedback tailored specifically to the complex electrical and thermal behavior of SiC and GaN transistors. In Figure 15, an example of a digital twin configuration for a power converter is illustrated, with real-time of bidirectional data exchange between the physical converter and its virtual counterpart.

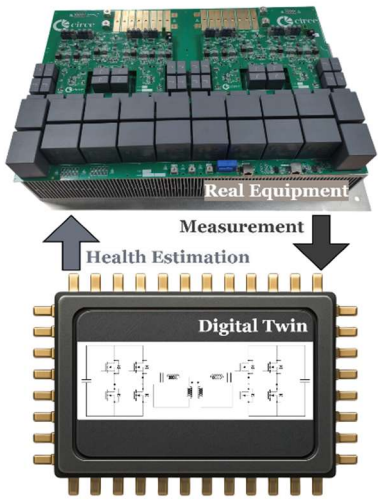

Figure 15: An example of a digital twin configuration for a power converter, with bidirectional data exchange between the physical converter and its digital replica.

In Figure 16, the hardware and solutions under development for implementing the converter's Digital Twin (DT) within the Flagchip project are presented. A dedicated PCB is mounted adjacent to the gate-driver board, which is called DT Measurement. This printed-circuit card acquires the driver-level measurements available to emulate the behavior of the power-electronic stage, and it can also establish a communications link with the main power-electronics controller to enrich the data set with additional converter-level information.

Upstream of the DT Measurement PCB it's the DT Edge Computer. Linked to the PCB via fiber-optic communication, this PCB performs two key roles: it aggregates raw measurement data into time-stamped packets and it enforces galvanic isolation between the high-voltage converter domain and the low-voltage control network. This edge platform executes the power-electronics digital twin in soft real time, using the incoming data to replicate the electrical-thermal behaviour of each module and to compute key health indicators, that act as quantitative markers of degradation. These indicators feed directly into lifetime-prediction algorithms, providing an up-to-date estimate of the remaining useful life of the power modules.

Furthermore, The DT Edge Computer is equipped with a dedicated communication interface that allows it to connect to an external server for comprehensive data management—both real-time status information and long-term historical records—and to an HMI platform, where operators can adjust model configurations and fine-tune parameters as required.

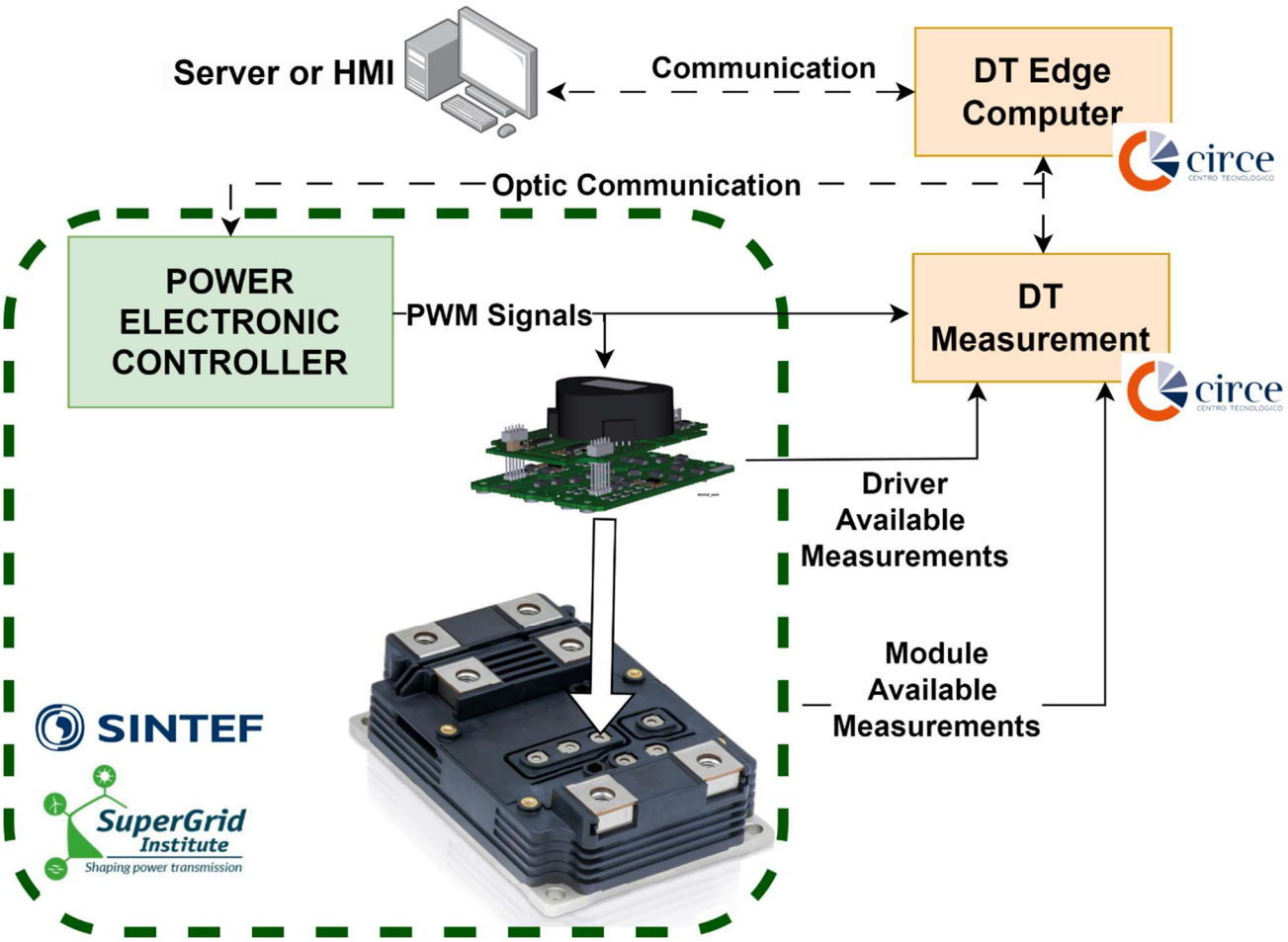

Figure 16: hardware solutions under development for implementing the converter's digital twin within the Flagchip project.

7. Conclusion

The developments presented in this report demonstrate significant advancements in Condition and Health Monitoring (C&HM) techniques for power electronic systems, with a particular focus on wide-bandgap devices such as SiC MOSFETs. Through a comprehensive evaluation of junction temperature estimation methods—including internal gate resistance probing, semiconductor TSEPs, and Fibre Bragg Grating (FBG) sensors—the project has laid the foundation for high-precision, real-time monitoring solutions. Each method has been critically assessed for its sensitivity, implementation complexity, and suitability for integration into commercial converter platforms. Notably, the power-cycling test bench developed for accelerated aging has enabled systematic degradation studies and validation of monitoring techniques under realistic thermal and electrical stress conditions.

Beyond sensing, the integration of a digital twin architecture marks a major leap forward in predictive maintenance strategies. The proposed framework enables real-time degradation tracking, lifetime extrapolation, and control adaptation based on health status—without requiring intrusive hardware. These capabilities are essential for high-reliability applications such as renewable energy systems, electric mobility, and aerospace. Together, the contributions from WP4 move beyond the state-of-the-art by combining advanced sensing, robust calibration, and embedded intelligence. The outcomes not only strengthen the FLAGCHIP project's technological ambitions but also provide a replicable path for future C&HM integration in power-electronic converters operating under demanding conditions.

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