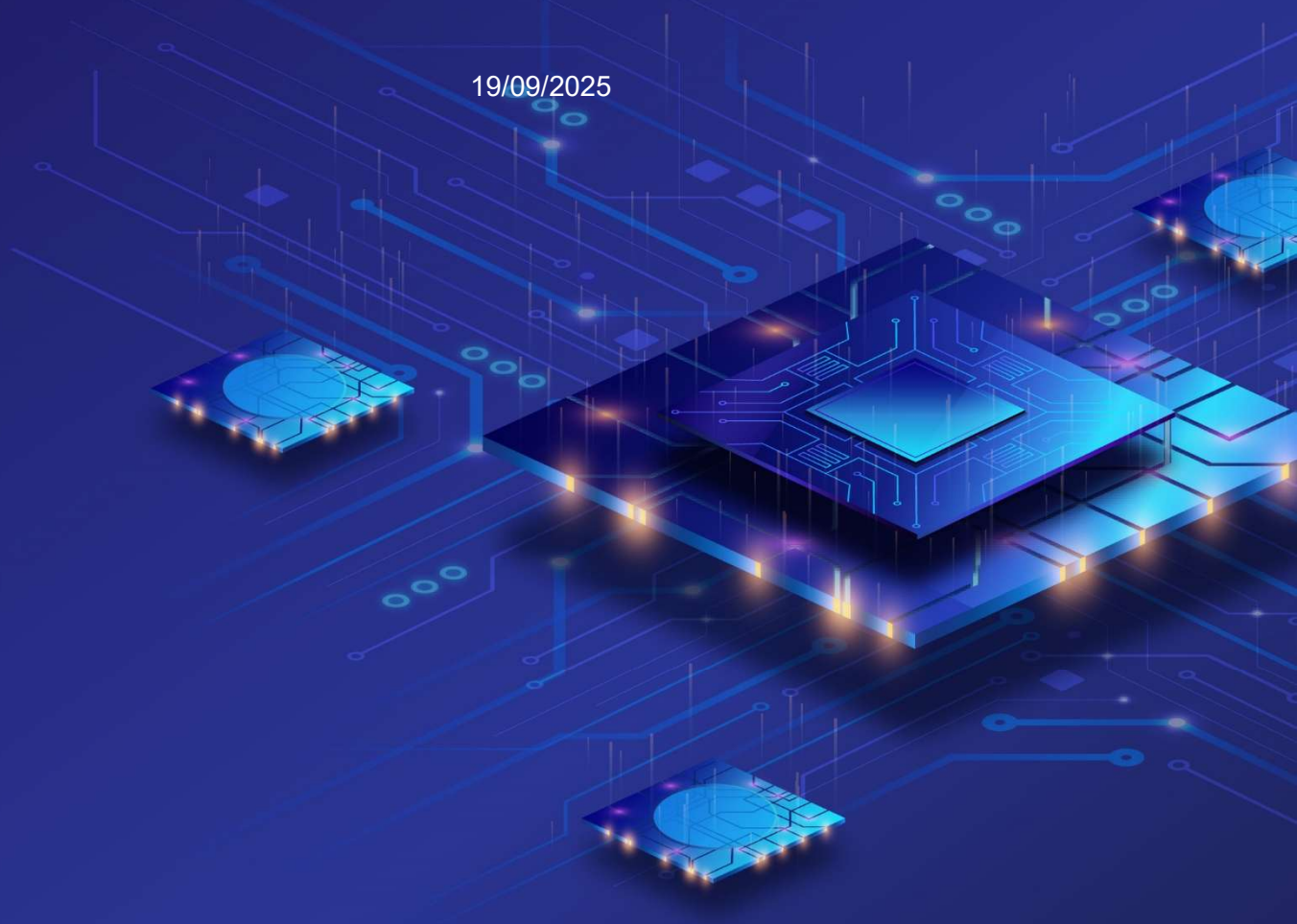
FLAGCHIP

FLAGSHIP SOLUTIONS IN POWER ELECTRONICS

D3.6 Public Report on Packaging and submodule topologies

INSA

19/09/2025



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Executive Summary

This report constitutes the first part of a 2-part document presenting the packaging and submodule structure developed as part of FLAGCHIP's work package 3. This first part mainly presents the state-of-the-art in packaging technologies for medium voltage power electronics, and presents possible development routes for the upcoming FLAGCHIP developments. Note that as it is intended for public release, it does not constitute an exhaustive report of our progress in FLAGCHIP.

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Table 1. Terms and Definitions

Abbreviation	Definition
MVDC	Medium Voltage DC

UWBG	Ultra-WBG
SiC	Silicon Carbide
R_{DSon}	State resistance
MMC	Modular Multilevel Converter
PEBB	Power Electronics Building Block
R_{thJA}	Ambient thermal resistance

1. Introduction

1.1 Context

The efficient collection and transport of renewable energy require Medium Voltage DC (MVDC) networks [Le Metayer 2021], which typically operate at bus voltages ranging from 5 to 50 kV. Such MVDC networks are based on power electronics converters (for AC-DC conversion, as well as to step voltage levels up or down).

Wide-bangap (WBG) semiconductor materials allow the design of power devices (transistors, diodes) rated at 6.5 kV, 10 kV or more [Palmour 2014], which are particularly well suited to MVDC converters. Among the various WBG and Ultra-WBG (UWBG) materials, Silicon Carbide (SiC) currently offers the most mature technology.

While the development of SiC devices towards higher voltages remains an active research topic, another key issue for their integration in MVDC converters is the design of efficient, reliable, and cost-effective packaging solutions. This section provides an overview of the technologies and approaches which can be used to package high voltage SiC chips to form power modules.

Note: while the term "Medium-Voltage" is commonly used when referring to networks, power semiconductor devices rated 3.3 kV and more are designated as "high voltage". As a consequence, in this report, the terms "high voltage" and "medium voltage" are used interchangeably.

1.2 State of the art of high voltage module technology

1.2.1 Module topology

Power modules come in a broad range of possible circuit topologies: some only feature a single switch (transistor, diode), some a half-bridge or even a 3-phase inverter circuit. Some power module also include auxiliary features such as gate drivers, sensors, etc. One key aspect of FLAGCHIP's investigations is the identification of the topology which is most suited to high voltage.

Indeed, integrating as many features in a single package may help in the management of high voltages and allow for a more compact converter. However, it may also result in less flexible designs, or present challenges in terms of reliability, manufacturing yield, or cost.

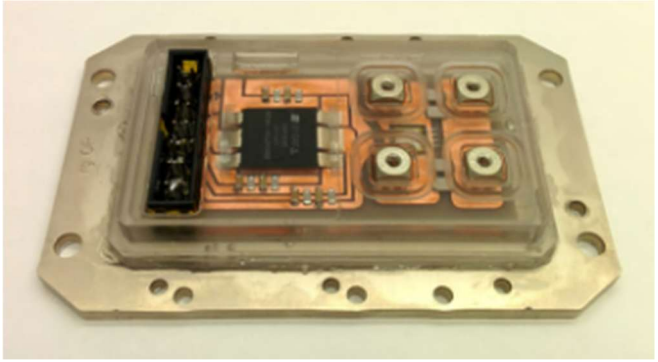

Figure 1: 10kV single-chip power module including the output buffer stage of the gate driver, for high frequency operation (1 MHz) [Jorgensen 2019

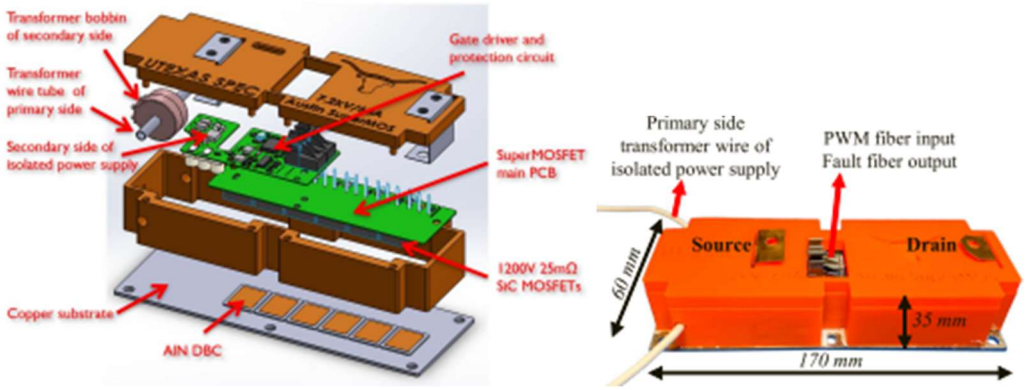

Figure 2: 7.2 kV 60 A, single-switch IPM, including 6 SiC MOSFETs (1.2 kV-rating) in a series configuration ("Super-MOSFET"), their associated gate driver and balancing circuit, gate drive power supply (with inductive energy transfer), and fibre optics communicat

In recent years, several research groups have proposed high voltage power module which in many cases go beyond the mere integration of power semiconductor devices in a package. For example, [Jorgensen 2019] integrated a gate driver circuit on the same substrate as a 10 kV SiC MOSFET to enable operation at up to 1 MHz (Figure1), forming the high voltage equivalent of the “intelligent power modules” which are commonly found with ratings of 650 or 1200 V.

A more complete example, also based on 10 kV MOSFET is presented in [Wang 2018]: it includes a full bridge topology, a capacitor, the associated gate driver circuits and auxiliary power supplies, some sensors, and a controller board to form a 6 kV submodule, the basic building block of an Modular Multilevel Converter (MMC). This extremely integrated approach is typically referred to as a Power Electronics Building Block (PEBB) [Ericsen 2006].

Because high voltage semiconductor devices remain difficult to procure, and may remain expensive, an interesting approach is the series connection of lower voltage devices. This, however, requires special care in the implementation to ensure balanced voltage sharing between individual devices [Mathieu de Vienne 2023]. Therefore, it is interesting to integrate the series-connected devices and their auxiliary components in a single module, as depicted in Figure 2 [Zhang 2020] or in Figure 3 [Al-Hinaai 2024] (also discussed below).

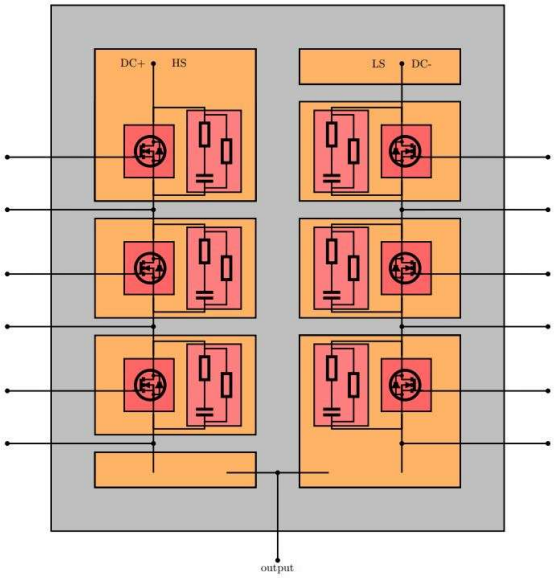

Figure 3: Circuit diagram for a half bridge with 3 chips connected in series per switch position, and their associated RC snubber [Al-Hinaai 2024]

1.2.2 Module technology

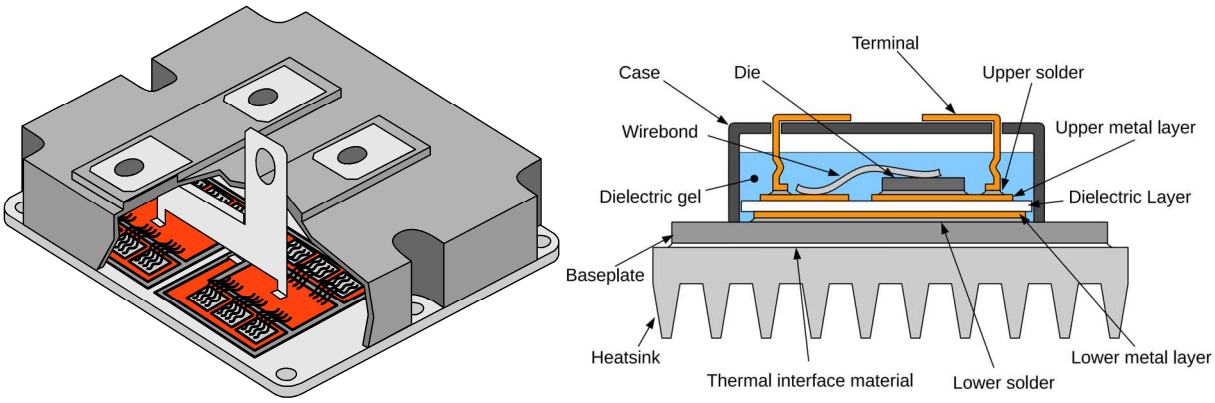

Figure 4:Typical power module, based on established packaging technology [own work]

A review of high voltage module technologies is available from [Li 2024]. It shows that the vast majority of SiC commercial products is currently centred on 3.3 kV modules. Most modules rated 6.5, 10 kV or more are still at the lab level. Furthermore, with one exception ([DiMarino 2017], discussed later below), all these modules rely on solid insulation and cooling through a separate heat exchanger (heatsink, cold plate…). Typically, they use variants of the structure depicted in Figure 4, in which the power semiconductor devices are attached to a metal/ceramic substrate. The ceramic layer provides electrical insulation, while offering a relatively high thermal conductivity for the thermal management of the power devices. The substrates are then attached to a metal baseplate (which is then bolted on the external heat-exchanger). In addition to the ceramic layer, electrical isolation is ensured by an encapsulant (typically silicone gel) and a plastic case.

While the power module structure from Figure 4 is well established (with variants in the materials or manufacturing technologies), it is intrinsically limited in its capability to reach high voltages: increasing the breakdown voltage of the ceramic substrate means making it thicker. This, however,

also increases its thermal resistance. Therefore, there is a competition between operating voltage and thermal management. This problem is especially acute as the breakdown voltage does not increase linearly with the ceramic thickness (because of electric field reinforcement issues discussed later), and because the performance of high voltage SiC devices drops rapidly when their junction temperature increases [Buttay 2018].

Because of this fundamental electrical/thermal trade-off, both aspects are discussed below in their own sub-sections.

1.2.3 Electrical isolation

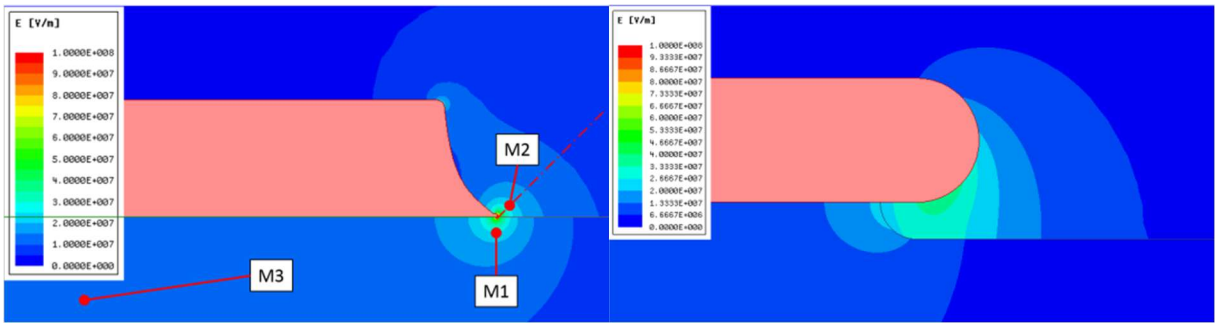

Figure 5: (left) Cross section of a ceramic substrate, showing the "triple point", at the interface of the ceramic (bottom layer), the copper electrode (salmon-coloured area) and the encapsulating material (top-right). This triple point is both the location of a

Because of the way they are manufactured, the metal/ceramic substrates cause strong electric fields to appear (Figure 5), regardless of the ceramic thickness. Such localized electric fields can exceed the breakdown field of the ceramic (typically AlN) or or the encapsulating material (typically silicone gel). Alternative approaches have been explored to propose different geometries [Reynes 2017, Hourdequin 2019, DiMarino 2017]. They demonstrate significant improvements over partial discharge inception voltages (PDIV) and/or breakdown voltages (in the range of a few tens of percent), but this remains limited. Furthermore, such geometrical modifications involve a complete change in the way the ceramic substrates are manufactured, which is impractical. In any case, it remains difficult to produce PD-free substrates for 10 kV and above.

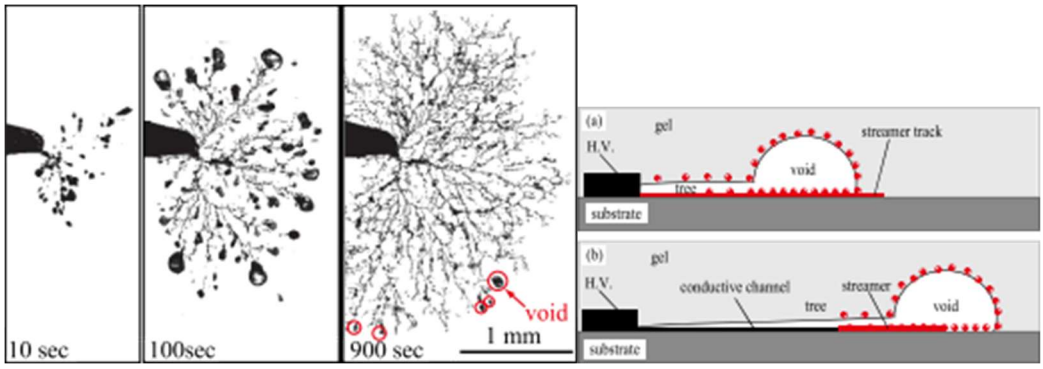

Figure 6: (left) Propagation of cavities in a silicone gel on glass substrate due to partial discharges, as a function of time, at 8 kV, 50 Hz. (right): model for the propagation of the cavities on glass (top) and AlN (bottom). In this latter case, PDs form a co

Partial discharges are especially concerning when they develop in the encapsulating material, as they cause accumulation of damage, eventually resulting in the breakdown of the isolation (Figure 6). [Auge 2013] shows that such partial discharges typically initiate at the triple point, and develop in the silicone gel. As for the substrates, workarounds have been proposed, such as filling the edges of the metallizations with an epoxy resin that can withstand a stronger electric field [Waltrich 2016], or with a resin loaded with non-linear resistive particle to attenuate the field reinforcement [Donzel 2012]. But here again, the effect remains limited and has strong consequences on the manufacturing process.

HV SiC devices will require special attention with respect to stable blocking performance under harsh environmental conditions (e.g. humidity) by utilizing optimum termination designs and dimensions to take into account the effects inside and outside the chip [Infineon 2020]. Further improvements are also required in the chip passivation and packaging encapsulation materials for the further device protection. In particular, the package chip protection capability is key for long term blocking stability under harsh environmental conditions especially if humidity-prone filling materials are employed such as Silicone Gel compared to other materials such as epoxy mold or hermetic packaging which represent more robust solutions

In consequence, it appears that increasing the operating voltage of power modules beyond 10 kV requires fundamental change in their structure. Furthermore, this re-design must take the manufacturing processes into account, to make sure the resulting design is compatible with existing material and processes.

1.2.4 Thermal management

High voltage SiC MOSFETs become relatively inefficient as their junction temperature (T_J) increases. This is because their on-state resistance (R_{DSon}) increases steeply with the temperature (up to 3-fold increase between 25 and 175°C). In consequence, it has been demonstrated in [Reynes 2027b] that these devices should be used at a T_J of 100°C or less. This is a fairly demanding objective, as such devices typically operate at a power loss density of 200-400 W/cm² at chip level.

As a consequence, a very low junction-to-ambient thermal resistance (R_{thJA}) must be provided to these devices. For example, in [Al-Hinaai 2024], an objective of 0.5 K/W is set, so that 3.3 kV SiC MOSFETs can operate at 120 W power dissipation at a 40°C ambient without exceeding 100°C T_J.

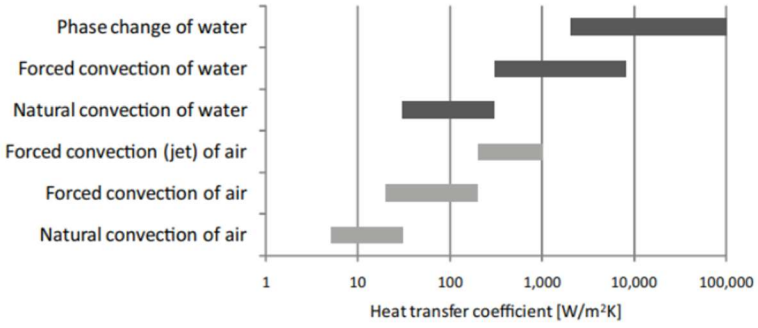

Figure 7: Ranges of heat-exchange coefficient values for various heat-removal techniques. Document from A. Bejan, "Heat Transfer," John Wiley Sons, Inc., New York, 1993 cited by [Ahmed 2024]

To reach such a low R_{thJA}, the package must first ensure the heat dissipated by the chip is efficiently spread over a larger surface (so as to reduce the heat density and facilitate extraction). This is typically done using high thermal conductivity materials such as copper and aluminium nitride (AlN) for the isolating layer. Then the package must provide a heat path to remove heat to the environment. Even with proper spreading, power density remains in the order of 10-50 W/cm² (100-500 kW/m²). This in turn means heat-exchange coefficient between the outer boundary of the module and the heat-carrying fluid must be in the order of 10-100 kW/(m².K).Figure 7 shows that such heat-exchange coefficients can only be achieved using liquid cooling (ideally with water), and that air-cooling is not suitable.

High voltage systems, such as Hvdc converters typically use deionised water as the cooling fluid. While this is efficient from a heat-transfer point-of-view, it requires continuous filtering to ensure the water remains deionised (and therefore electrically insulating). Recently, many studies have focused on alternative dielectric fluids. These offer the advantage of not requiring continuous filtration. Furthermore, some of them have a low boiling point, allowing to take advantage of the high heat-exchange coefficient offered by phase change [Saums 2010]. Most of these studies have focused on fluorinated fluids [Iradukunda 2020] (hydro-fluoro-ethers), which have satisfying thermal performance, low accute toxicity, and relatively good environmental performance regarding their global warming potential or their effect to the ozone layer. Passive systems have been proposed, in which the motion of the cooling fluid is caused by the difference in density between the liquid and vapour phases [Moustaid 2022], simplifying the cooling system further.

While diphasic systems can offer more thermal performance, single-phase cooling systems base on dielectric fluids have also been proposed. In [Al-Hinaai 2024], a ceramic heat-exchanger is introduced, which is used with a dielectric fluid. While the performance with the dielectric fluid is slightly lower than with water, it is still sufficient to operate SiC chips at more than 400 W/cm².

Indeed, the heat-exchange coefficient values displayed in Figure 7 are relatively conservative, and higher values can be achieved thanks to advanced management of the liquid flow. In particular, jet impingement, in which the cooling fluid impacts the heat-exchange surface at a right angle ensures good mixing of the fluid and allows for reaching heat-exchange coefficients of approximately 20-50 kW/(m².K) [DiMarino 2017, Ahmed 2024, Al-Hinaai 2024]. Other approaches are also possible, such as channel flow with pin fins [Jorgensen 2023, Al-Hinaai 2024]. [Iradukunda 2020] provides a comprehensive overview of high-performance fluid and cooling configurations.

While hydro-Fluoro-ether fluids were marketed as healthy and environmentally conscious, it has recently become apparent that the class of chemical they belong to (Per- and polyfluoroalkyl substances, or PFAS) is extremely pervasive in the environment and where it has a very long life (hence their nickname of “eternal pollutants”). As a consequence, this class of fluid is phased-out by some manufacturers and should now be avoided. Some studies investigate the use of fluoride-free dielectric fluids, such as the oils used in high voltage transformers. For example in [Le Metayer 2022], a diode rectifier is immersed in a synthetic ester oil (Midel 7131) and cooled by natural convection. One of the few examples of forced convection cooling of power electronics using a transformer oil is [Schnur 2018]. In this paper, a relatively small R_{thJA} of 0.52 K/W is achieved. The limited thermal performance of transformer oil (when compared with water) is counterbalanced by the removal of the insulating layers (ceramics or organic insulator), the insulator being the cooling oil itself. Such an approach, in which some [Buttay 2017] or all [Schnur 2018] of the electrical

insulation is supplied by the cooling fluid is a very attractive solution to overcome the electrical/thermal trade-off discussed previously.

1.3 Objectives

The objectives of FLAGCHIP's WP3 is to develop a 10kV module using technologies that are compatible with a further increase in voltage, and which allow to fully exploit the performance of high-voltage SiC MOSFETs.

These packaging technologies should allow to build a multi-chip (parallel and series connection) module, and the integration of auxiliary features (sensors, signal conditioning, etc.) while keeping the module as compact as possible.

2. Submodule Topologies

2.1 Submodule topologies for a 10 kV bridge

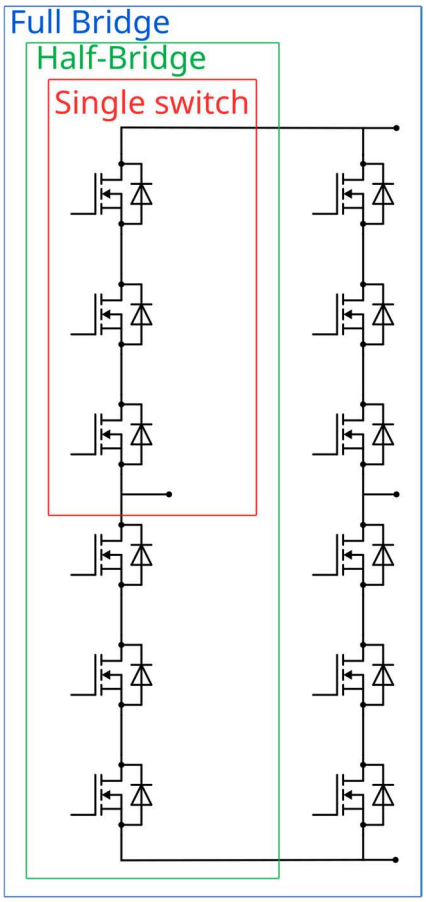

Figure 8: 10 kV full bridge inverter, depicting the 3 ways type1 modules can be implemented

According to the specifications of FLAGCHIP's pilots, a 10 kV full-bridge must be formed with the power module(s). Because 6.5 kV SiC MOSFET chips will be integrated in the module, and used with a 45% de-rating, 3 chips must be connected in series to form a 10 kV switch.

Depending on the implementation constraints (insulation distances, footprint of the chips and associated auxiliary elements), the power module topology may correspond to any of the 3 ways depicted in Figure 8.

3. Packaging technology

3.1 FLAGCHIP module concept

As discussed in the state-of-the-art section, a profound change in module architecture is required to simultaneously achieve high voltage, continuous operation and the low thermal resistance required by high voltage SiC devices.

The developments in FLACGHIP will focus on using dielectric fluids, as these allow to build cooling loops with low-maintenance, with a specific focus on fluids with low environmental footprint.

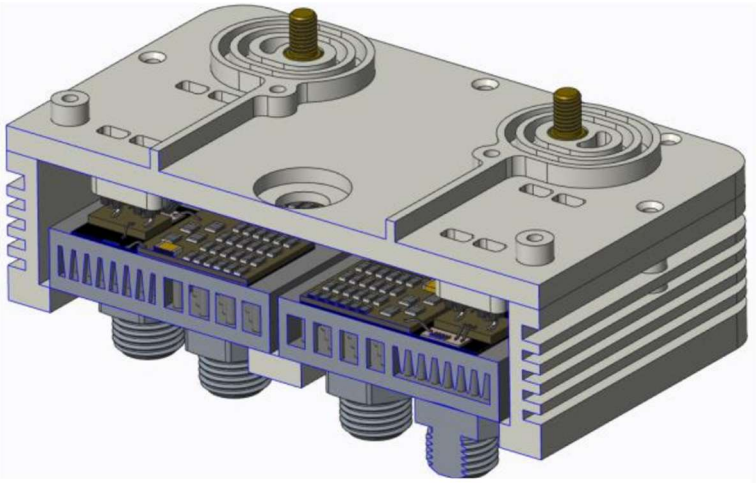

Figure 9: Module structure based on a ceramic heatsink, in which a dielectric fluid flows [Mathieu de Vienne 2023]

One possible solution is to build upon the structure developed in [Al-Hinaai 2024, Mathieu de Vienne 2023], and which is depicted in Figure 9. Here, the electrical insulation is provided by both the ceramic heatsink and the dielectric cooling fluid. The limitations of this approach are:

- the thermal conductivity of the ceramic heatsink: while a high performance AlN ceramic was used, its thermal conductivity is still less than half that of copper, which limits heat spreading and evacuation;
- the insulating performance of the encapsulation material (a silicone gel, not depicted in Figure 9).

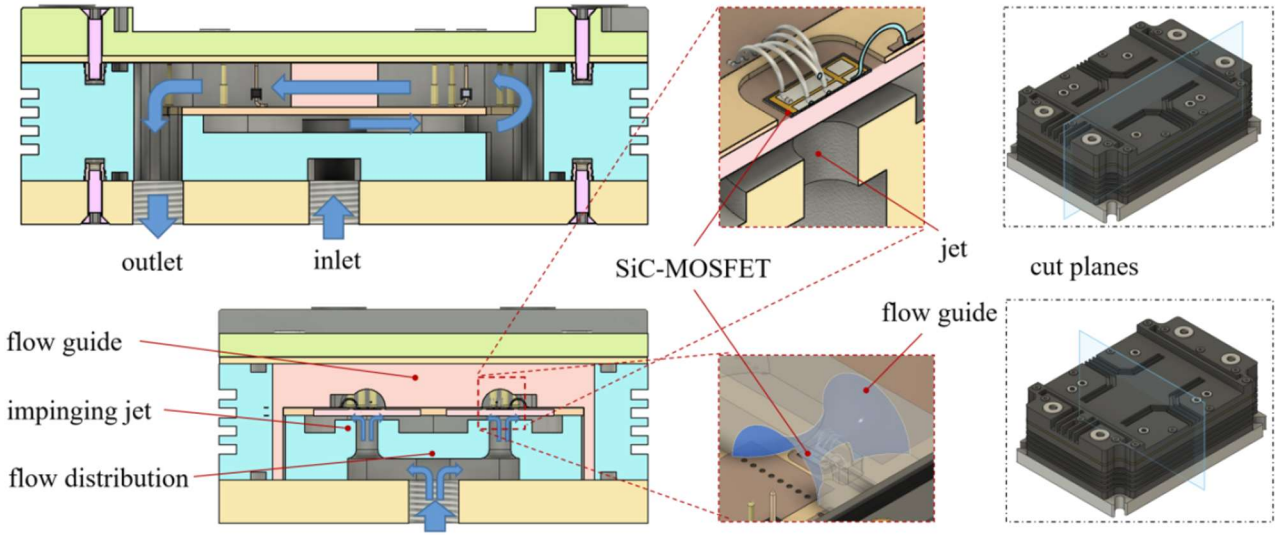

Figure 10: Structure of power modules with dielectric fluid for cooling and isolation [Huesgen 2025]

Another possibility is to remove the ceramic layer entirely, in a structure akin to that presented in [Huesgen 2025] (Figure 10). The concept is based on a dielectric liquid that is used for both, cooling and insulation. The semiconductor chips are attached to Cu inlays in a PCB substrate. Dual side cooling is achieved by jet impingement on the bottom side and immersion in the dielectric liquid on the top side.

4. Conclusion

This report has presented a review of the approaches that have been used to design high voltage power modules. This allowed to identify the most relevant routes for the design of FLAGCHIP's power modules. In particular, dielectric fluid cooling has been selected, and bottleneck have been identified with the silicone gel encapsulation.

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