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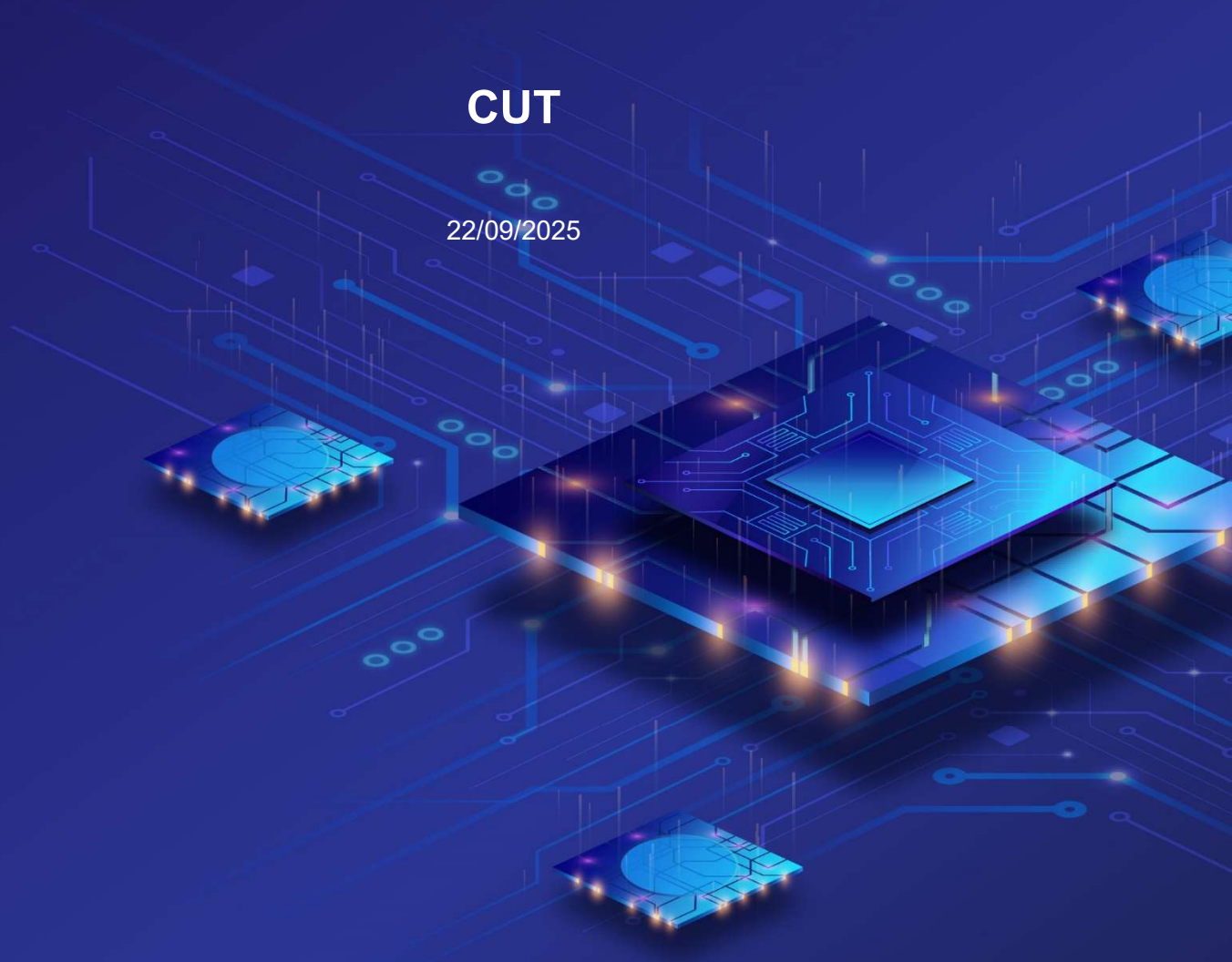
D2.2 Reliability models for SiC MOSFETS and UWBG

CUT

22/09/2025



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Executive Summary

In this deliverable report, research progress in terms of SiC-MOSFET reliability characterisation and modelling in WP2 of the FLAGCHIP project is presented. Characterisation methods of a 3.3kV SiC-MOSFET device and module from Hitachi Energy are first described. The characterisation results can be used to parameterize the SiC MOSFET TCAD and behavioural models as well as their validation. Afterwards, a SiC MOSFET TCAD model is presented and will be calibrated using the above characterisation results. The TCAD model allows us to study the origin of instabilities and shifts in parameters, the physics of the failure and to extract the unmeasurable parameters (such as channel current, the voltage across the gate oxide), which will be crucial to understand semiconductor devices physics for improvement. As TCAD simulation is computationally demanding and therefore slow for circuit and power converter simulation, a SiC-MOSFET behavioural model is proposed and developed to address the challenge. A series of RC network are used to model the time-constant of the parameter drift, which represents their aging with operation conditions. The extracting of the parameters needed in the behavioural model will be based on curve fitting using both device reliability characterisation results and TCAD simulation results. The behavioural models will then be provided to WP4 to enable representative remaining useful lifetime estimation and health estimation within the real-time simulation of power electronics digital twin.

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Abbreviation	Definition
BIT	Bias Temperature Instability
C_{RSS}	Reverse Capacitance
$R_{DS(ON)}$	Drain-source on-state resistance
C_{OSS}	Capacitance Output
C_{ISS}	Capacitance Input
C_{RSS}	Capacitance Reverse
T_{CASE}	Case Temperature
SC	Short-circuit
OLTO	Overload turn-off switching
UIS	Unclamped Inductive Switching
TCAD	Technology Computer-Aided Design
UWBG	Ultra-Wide Band Gap

Table 1 Terms and Definitions

1. Objectives of this document

This report presents the updated characterisation and modelling work of SiC-MOSFET reliability in WP2 of the FLAGCHIP project. The document will be updated by M30 to include the research work of ultra-wide bandgap devices (UWBG), which will start from M13 (September 2025).

2. Introduction

Power semiconductor devices modelling is crucial for power converter design and validation before prototyping, which saves the designers' time and development cost. With regards to reliability modelling, it is important to understand their lifetime and physics of failure by considering their application scenarios, which is one of the aims of the research activities carried out in WP2.

The SiC-MOSFET used in WP2 is a 3.3kV device from Hitachi Energy. The current rating of each chip is about 25A. The same devices are used in a half -bridge 3.3kV 500A LinPak module manufactured by Hitachi Energy. In order to evaluate device reliability, a few reliability tests are carried out for both chips and power modules. To understand device reliability and physics of failure, semiconductor device Technology Computer Aided Design (TCAD) is used, which offer good insights on device physics and help to accelerate the experimental characterisation time. To propose a reliability model useful for remaining useful lifetime prediction of a power converter digital twin (other research activities being carried out in WP4), a behavioural model is developed for power converter simulation.

The deliverable report summarises our research work until M13 (September 2025) of the FLAGCHIP project, and the report is structured with following sections: Section 3 presents the SiC-MOSFET characterisation method. Section 4 presents device TCAD simulation results. Following that, a SiC-MOSFET behavioural model is presented in Section 5. The report is concluded in Section 6.

3. SiC-MOSFET characterisation

This project also involves performing electrothermal static and dynamic device characterisation of various types of project-relevant 3.3kV rated SiC Power MOSFETs in single discrete **bare die** chip and **TO-247-4L** package as well as **LinPak** half H-bridge / phase-leg module. Here, the aim of device characterisation is to have an in-depth set of experimental results at various test conditions (i.e. input voltage (V_{DD}), case temperature (T_{CASE}), switching current (I_{SW}) etc.) to complement and improve the behavioral and TCAD modelling work in this work package WP2. The static characterisation of power devices would be performed using the state-of-the-art B1505A Curve Tracer equipment from Keysight. This equipment can provide all the typical information that one could find within the datasheet of a typical SiC MOSFET transistor commercially available on the market. The typical static characterisation tests that are of interest for our activities in this WP are as follows:

- Output Characteristics
- Transfer Characteristics
- 3rd Quadrant Characteristics
- Body-diode Performance
- Drain-source on-state resistance ($R_{DS(ON)}$)
- Capacitance (Input (C_{ISS}), Output (C_{OSS}), and Reverse (C_{RSS}))
- Reverse blocking and leakage current

Selected test results showing the output characteristics at case temperature (T_{CASE}) = 25°C of a phase leg power module are also presented here in Figure 1 below.

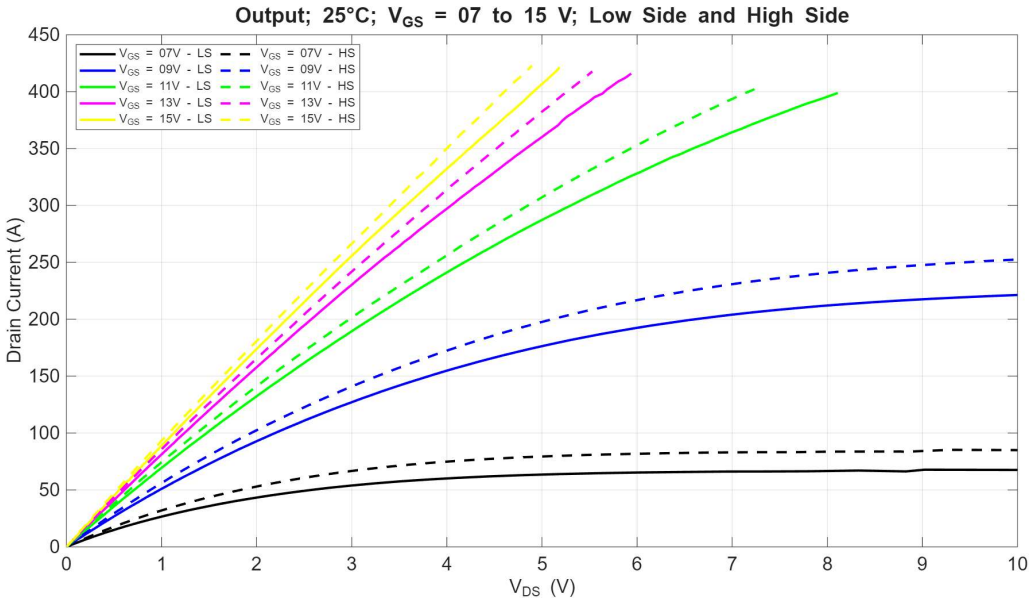

Figure 1: Output characteristics of the 3.3 kV SiC MOSFET phase leg module

Moreover, switching dynamic device performance is equally important which is performed using a dedicated and bespoke double pulse tester (DPT) board. A detailed device characterization case

study is important to determine the device operating behavior within its safe operating area (SOA), as well as to know their limits under unintended abnormal operational modes outside of the SOA. Nevertheless, such stressful outside of SOA operational modes are of frequent occurrence within real applications. The possible dynamic tests that can be performed on project devices for the needs of reliability model development are as follows:

- **Nominal Double Pulse Switching test** – This test is conducted to determine the turn-off and turn-on switching voltage and current transients of a transistor which then help to calculate the relevant turn-on and turn-off energies (E_{ON}) and (E_{OFF}) needed for loss calculations.
- **Gate Charge Q_G test** – This test is conducted to determine the gate charge value of the SiC MOSFET under switching conditions during turn-off
- **Short-circuit (SC) robustness** – This test is aimed to determine the short-circuit withstand capability (t_{SC}), usually within seconds, and the relevant energy dissipation (E_{SC}) during SC mode.
- **Overload turn-off switching (OLTO)** test – This test is performed by switching-off the transistor (in both MOSFET and Diode modes) at twice the nominal device current (I_D) rating to know the transistor's switching performance under overload conditions.
- **Unclamped Inductive Switching (UIS) test** – SiC MOSFETs are intrinsically avalanche rugged which gives them the ability to dissipate energy during avalanche (E_{AS}). This test has been designed to estimate the MOSFET's avalanche breakdown energy dissipation capability under different drain source voltages (V_{DS})and current (I_D) conditions.
- **Diode Surge Current test** – The SiC MOSFET internal bipolar diode is required to have a surge current withstand capability with a typical half-sine pulse having an amplitude of around 10 x times the nominal current and a time interval of up to 10 milliseconds.

The typical schematic of a DPT circuit is shown in Figure 2. A dedicated PCB has been designed and manufactured as presented in Figure 3 below. Some adjustments would be needed to be made between point A and B as indicated in the schematics to alter the test setup designed to select the test type being carried out.

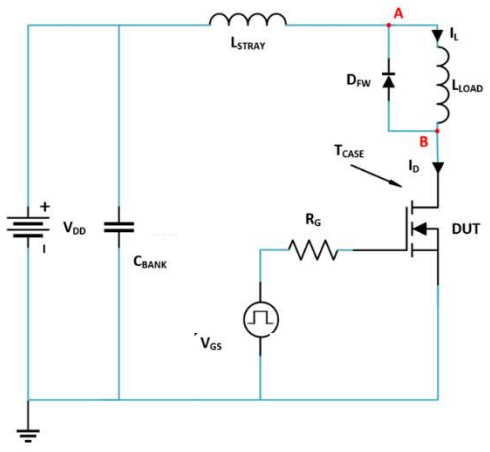

Figure 2: Dedicated PCB for dynamic switching tests for FLAGCHIP project

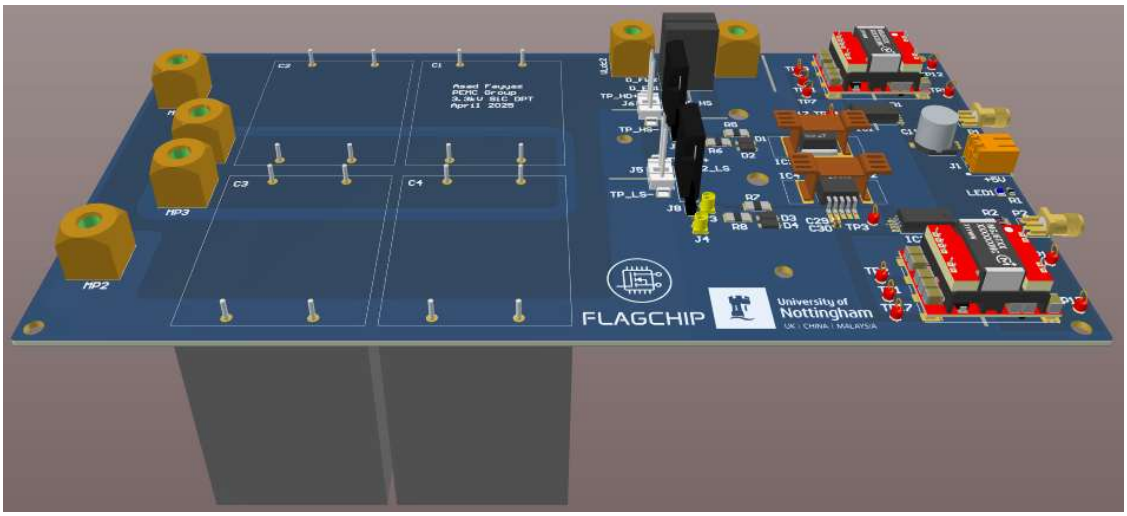

Figure 3: Dedicated PCB for dynamic switching tests for FLAGCHIP project

Furthermore, other tests to investigate the reliability of different features of a SiC MOSFET, such as the gate-oxide reliability and body-diode reliability, are also of relevance of here. Some of these tests which could be performed on the project devices are:

- **High temperature gate bias (HTGB) test** – This test is designed to stress the gate oxide reliability by applying DC bias (V_{GS}) to the gate source terminals at high temperatures to check to threshold voltage instabilities (over a 1000 hour time range) due to different types of gate oxide traps.
- **High temperature reverse bias (HTRB) test** – Here, the device is DC biased (V_{DS}) between the drain and source terminals under high T_{CASE} to evaluate the device's long-term stability by continually monitoring the drain leakage current (I_{LEAK}) over 1000 hours.
- **High temperature forward bias (HTFB) test** – The objective of this test is to investigate defects in the SiC wafer and the p-n junction that could cause a shift in the body diode's on-state voltage drop. In this test, the intrinsic body diode of the device is forward biased by applying a voltage between the source and drain while keeping the gate-to-source voltage $V_{GS} \leq 0$. The forward voltage (V_F) of the body diode is measured at regular intervals to monitor any variations in its electrical characteristics over time.

The list of test methods presented here discusses the most used techniques to characterise power devices. Nonetheless, the list presented here is quite exhaustive but not complete and other tests also exist which are not of direct importance for the project's needs. We reference here Infineon white paper which takes into consideration a number of reliability related tests with clear focus on SiC MOSFETs[1]. Hence, other techniques would also be studied and implemented if needed for the work being carried out in WP2.

[1] Infineon White Paper "How Infineon controls and assures the reliability of SiC based power semiconductors", July 2020.

4. SiC-MOSFET TCAD model

4.1 Purpose and Role of TCAD in FLAGCHIP

Technology Computer-Aided Design (TCAD) simulations are employed in FLAGCHIP to understand and predict the internal physics of SiC MOSFETs, and to support the development of reliable and optimised device designs. These models provide a physically grounded framework to assess performance and reliability under realistic operating conditions.

4.2 Modelling Challenges in SiC Devices

Compared to silicon, SiC introduces unique challenges in TCAD due to its wide band-gap and high critical electric field, which impact breakdown behaviour, incomplete ionisation of dopants, and strong temperature dependence of both drift and channel transport. Furthermore, the SiC/SiO_2 interface contains a high density of electrically active defects, leading to degradation of channel mobility and threshold voltage instability. These factors necessitate rigorous selection and calibration of physical models, particularly for mobility and interface physics.

4.3 Interface and Trap Modelling

The performance of 4H-SiC MOSFETs is strongly affected by defects in the SiO_2 gate oxide and at the SiC/SiO_2 interface. Key contributions include:

- **Fixed Oxide Charge (Q_f):** Immobile charges located within the SiO_2 layer, typically positive for thermally grown oxides on SiC. Shift the threshold voltage and modify the electric field distribution in the channel.
- **Interface Traps (D_{it}):** Energy states located precisely at the SiC/SiO_2 boundary, which can exchange charge with the channel depending on bias and temperature. Distributed across the bandgap, often modelled with Gaussian or U-shaped energy distributions.
- **Near-Interface Oxide Traps (NIOTs):** Defects located within a few nanometres of the interface inside the oxide. Can communicate with the channel through tunnelling, influencing mobility and bias-temperature instability (BTI) behaviour.

In the TCAD model, both fixed charges and distributed interface traps are included, with parameter values chosen within literature-reported ranges. This allows the reproduction of threshold-voltage shifts, subthreshold slope degradation, and inversion-layer mobility reduction observed in experiments, while retaining flexibility to represent different foundry processes.

Typical ranges reported in literature for 4H-SiC MOS capacitors include[2][3][4][5][6]:

- Fixed Oxide Charge (Q_f) density: 1×10^{11} – 1×10^{12} cm^{-2}
- Interface Traps (D_{it}) density: 5×10^{11} – 5×10^{12} cm^{-2} eV^{-1}
- Trap centroid (E_{mid}): 0.03 – 0.08 eV below conduction band (E_c)
- Energy spread (σ): 0.05 – 0.15 eV

4.4 Mobility Modelling Framework

Carrier mobility is central to accurate prediction of MOSFET performance. In our TCAD implementation, the effective channel mobility (μ_{eff}) is expressed through Matthiessen's rule, which combines contributions from multiple scattering mechanisms:

$$\frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{\text{bulk}}} + \frac{1}{\mu_{\text{SR}}} + \frac{1}{\mu_{\text{SP}}} + \frac{1}{\mu_{\text{RCS}}}$$

where:

- μ_{bulk} = bulk mobility in the inversion layer
- μ_{SR} = mobility limited by surface roughness
- μ_{SP} = surface phonon scattering
- μ_{RCS} = remote Coulomb scattering due to interface and oxide charges

4.5 Bulk Mobility Modelling and Validation

Accurate modelling of bulk mobility in 4H-SiC is essential for predicting conduction in drift regions of high-voltage MOSFETs. The baseline model available was identified insufficient for wide band-gap materials, particularly in capturing temperature and doping dependence. As a result, a revised mobility model has been adopted and recalibrated for 4H-SiC, using Hall-effect datasets from Kimoto and Cooper as reference. This formulation incorporates lattice, ionised-impurity, and carrier–carrier scattering, providing accurate degradation trends at high doping and therefore applicability across a wide envelope of device doping profiles. It also sets the correct trend for correct temperature scaling up to elevated temperatures (> 400 K), with the parameterisation to be done and validated in the next step.

[2] Saks, N. S., et al. "Interface traps and oxide charges in thermally oxidized 4H-SiC." *IEEE Transactions on Electron Devices*, 46(3), 1999, pp. 456–464
[3] Saks, N. S., et al. "Interface traps and oxide charges in thermally oxidized 4H-SiC." *IEEE Transactions on Electron Devices*, 46(3), 1999, pp. 456–464
[4] Afanasev, V. V., et al. "Intrinsic SiC/SiO_2 interface states." *Physica Status Solidi (a)*, 162(1), 1997, pp. 321–337.
[5] Okamoto, D., et al. "Improved inversion channel mobility in 4H-SiC MOSFETs with deposited gate oxide by controlling interfacial carbon." *Applied Physics Letters*, 96(20), 203508, 2010.
[6] Dhar, S., et al. "Interface trap density and oxide reliability of thermally oxidized 4H-SiC MOS capacitors." *Journal of Applied Physics*, 97(3), 033706, 2005.

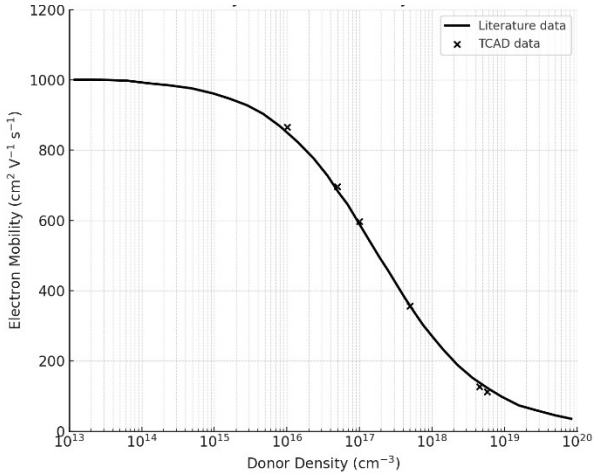

Figure 4: Comparison of TCAD model predictions against literature data[7], confirming close agreement over several decades of doping concentration at 300 K.

4.6 Electron mobility at the SiC/SiO_2 interface modelling and validation

Channel mobility in 4H-SiC MOSFETs is strongly degraded by interface defects. The model incorporates the scattering mechanisms listed above, calibrated against published measurements from lateral test structures. Parameters for each scattering term were iteratively tuned to ensure accurate gate-bias and temperature dependence. Validation results (Figure 5) demonstrate that the calibrated model reproduces experimental mobility trends across temperatures from 25 °C to 175 °C and doping levels between 3.6×10^{17} and 1.0×10^{18} cm^{-3}. This confirms the model's predictive accuracy in the operational space of FLAGCHIP devices.

[7] Kimoto, T., & Cooper, J. A. *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices, and Applications*. Wiley, 2014.

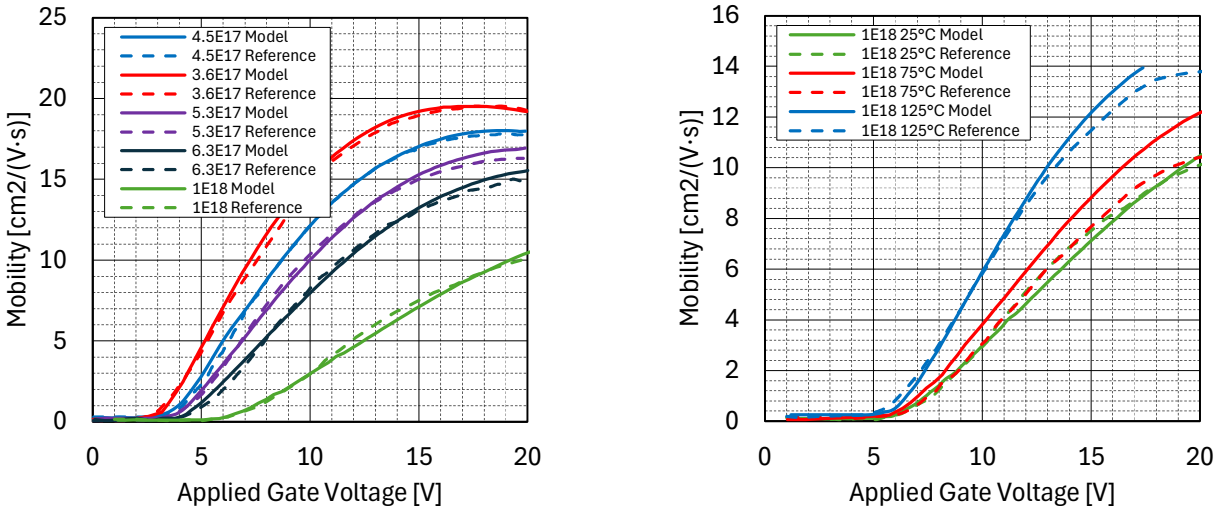

Figure 5: Doping and Temperature Dependency of inversion layer mobility of TCAD model showing good predicting ability compared to reference[8] values

4.7 Reference Device Setup

To support reliability studies and future device feature exploration, a planar 3.3 kV SiC MOSFET reference device has been established in TCAD. This structure represents a typical state-of-the-art technology node, providing a baseline against which new design concepts, degradation phenomena can be compared, and behavioural models can be developed. The reference geometry follows dimensions consistent with reported industrial practice and enables simulation of terminal behaviour under high-voltage stress conditions. The breakdown characteristics of the reference device are illustrated in Figure 6. These confirm that the chosen design space is aligned with the expected blocking performance of commercial-grade 3.3 kV devices.

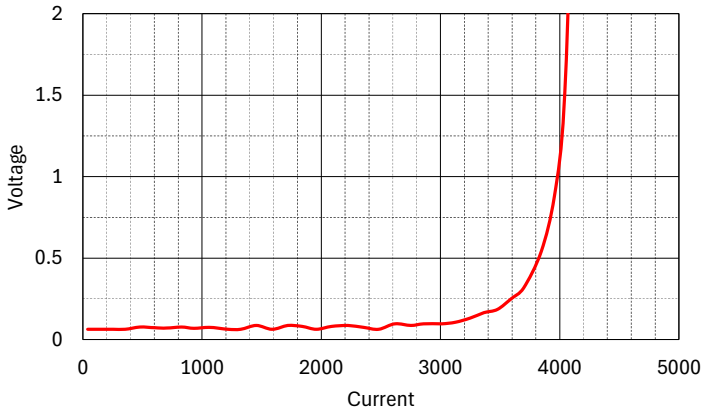

Figure 6: Simulated breakdown voltage of the 3.3 kV reference structure.

[8] H. Dixit, D. J. Lichtenwalner, A. Scholze, J. Kim, K. Han, and S.-H. Ryu, “Revised Channel Mobility Model for Predictive TCAD Simulations of 4H-SiC MOSFETs,” Solid State Phenomena, vol. 358, pp. 103–107, Aug. 2024, doi:10.4028/p-LaV11n.

By anchoring the simulations to this reference point, the TCAD framework can be used to evaluate degradation phenomena (e.g. mobility reduction, threshold-voltage instability) under controlled and realistic device conditions, develop compact behavioural models that reflect state-of-the-art device physics and benchmark emerging device concepts against established 3.3 kV performance levels.

4.8 Application to Reliability Modelling and Ongoing Work

The calibrated TCAD models provide a solid foundation for reliability-oriented simulations. These include predicting inversion-layer mobility degradation under stress, evaluating threshold voltage shifts associated with oxide charges and interface traps, and extracting local electric field and temperature distributions for use in higher-level reliability frameworks. The combined calibration of interface physics, channel mobility, and bulk transport within the TCAD environment offers a robust and predictive toolset for SiC MOSFET analysis. By linking these models to a 3.3 kV reference device benchmark, it establishes a reliable basis for studying degradation phenomena, supporting the development of reliability models, and informing future device innovations. Planned extensions will refine the treatment of degradation mechanisms and variability effects, but such details are not disclosed here as they remain the subject of ongoing research.

5. SiC-MOSFET behavioural model

A SiC-MOSFET behavioural model is presented in Figure 7, where there are mainly three parts:

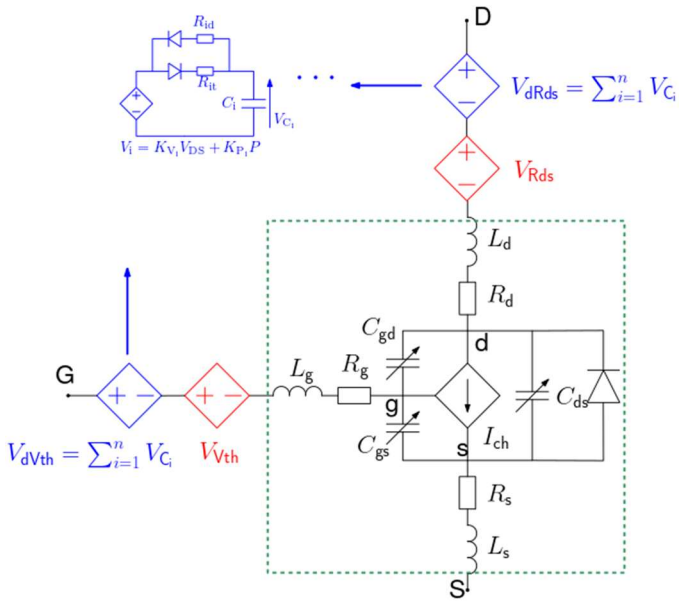

Figure 7: A SiC-MOSFET behavioural model proposed in FLAGCHIP to model device reliability

- Green dots. The classic transistor equivalent circuit represents its electro-thermal characteristics. The equivalent circuit is mainly formed by three parts: a controlled current source to represent MOSFET output characteristics, a body-diode to represent its reverse characteristics, three non-linear capacitances to model inter-electro capacitances and parasitic inductance and resistance due to device packaging. The used behavioural equations will be derived from our previous work, where the accuracy and validation of the model are shown in Figure 8 and Figure 9 for a 27kV SiC-IGBT and a 1.2kV SiC-MOSFET respectively.
- Blue parts. They are formed by controlled voltage sources to represent the instability issue of SiC-MOSFET (e.g. the threshold voltage hysteresis[9]). The trapping and detrapping time constants are modelled by respective RC circuits and these time constants could be obtained via device TCAD simulation. Some similar approaches have been presented for dynamic Rdson modelling of GaN-HEMT[10].
- Red parts. They are used to model permanent increase of leakage current, threshold voltage and ON-state resistance due to device aging. Their dependency on different stresses will be determined together by reliability characterisation and device TCAD simulation.

[9] Y. Cai *et al*., "Effect of Threshold Voltage Hysteresis on Switching Characteristics of Silicon Carbide MOSFETs," in *IEEE Transactions on Electron Devices*, vol. 68, no. 10, pp. 5014-5021, Oct. 2021, doi: 10.1109/TED.2021.3101459.
[10] Li, K.; Evans, P.L.; Johnson, C.M.; Videt, A.; Idir, N. A GaN-HEMT Compact Model Including Dynamic RDSon Effect for Power Electronics Converters. Energies 2021, 14, 2092. https://doi.org/10.3390/en14082092

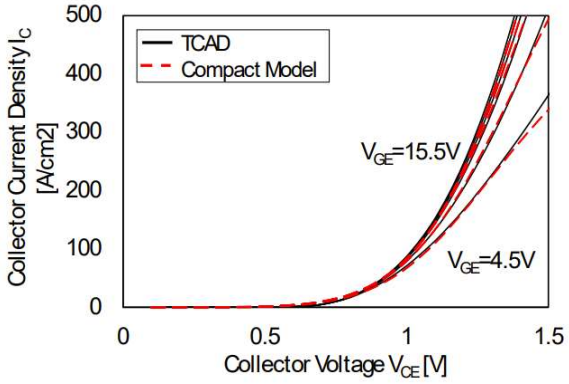

Figure 8: Case study of a 27kV SiC-IGBT[11]

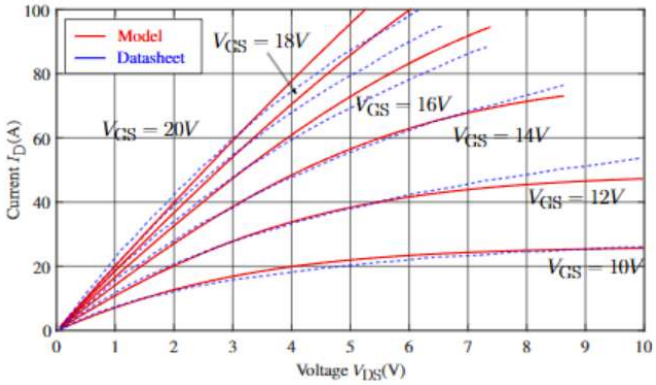

Figure 9: Case study of a 1.2kV SiC-MOSFET[12]

The presented behavioural model can be implemented into different power electronics simulation software such as LTspice, Simulink for power converter simulation, so the aging of device characteristics and their lifetime can be obtained by considering different application scenarios.

[11] I. Almpanis, P. Evans, K. Li and N. Lophitis, "IGBT Model for Circuit Simulations: Implementation of the Nonlinear Voltage-and Current-Dependent Capacitance Method to Silicon IGBTs," *2024 IEEE Design Methodologies Conference (DMC)*, Grenoble, France, 2024, pp. 1-3, doi: 10.1109/DMC62632.2024.10812174.

[12] K. Li, P. Evans and M. Johnson, "Using multi time-scale electro-thermal simulation approach to evaluate SiC-MOSFET power converter in virtual prototyping design tool," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, USA, 2017, pp. 1-8, doi: 10.1109/COMPEL.2017.8013278.

6. Conclusion

In this report, research progress of WP2 in SiC-MOSFET characterisation and modelling are presented. For reliability characterisation, a PCB has been designed to perform a various of switching reliability test. In terms of device reliability modelling, TCAD simulation was performed using a planar 3.3 kV SiC MOSFET reference device. TCAD simulation results such as trapping/detrapping time constants, and device characteristics degradations will be used to parameterise a proposed behavioural model for power converter simulation. We will continue the above research activities and update the deliverable report by M30.

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