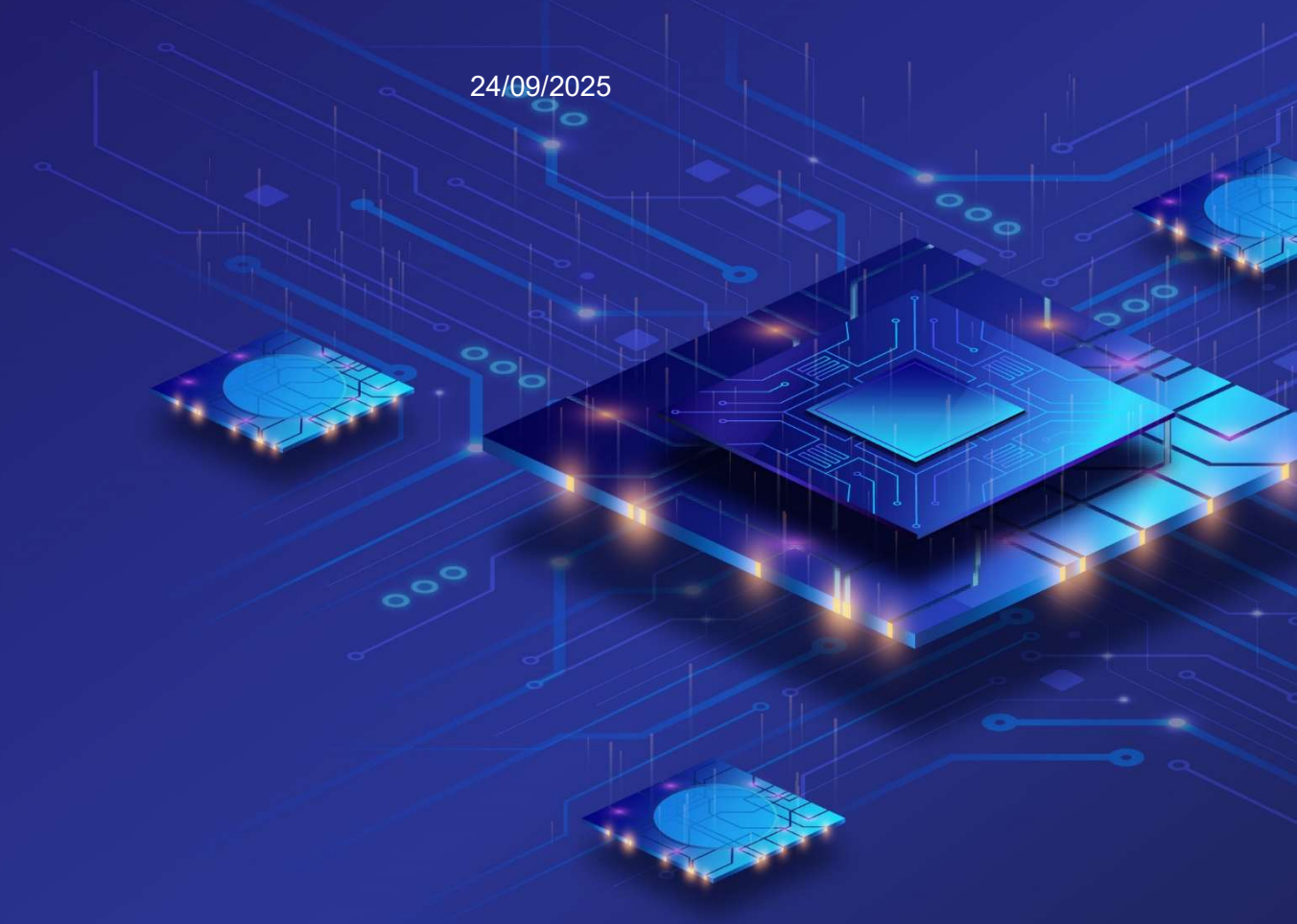
FLAGCHIP

FLAGSHIP SOLUTIONS IN POWER ELECTRONICS

D1.4 Project Progress Report

CIRCE

24/09/2025



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This project has used a standard methodology already developed in the Zhyron project (Grant Agreement number: 101138276). *Ad hoc* modifications were added to comply with the conditions of the Grant Agreement for FLAGCHIP project (Grant Agreement number: 101172794).

Executive Summary

FLAGCHIP is a 42-month Research and Innovation Action (09/2024 – 02/2028) funded by the European Climate, Infrastructure and Environment Executive Agency (CINEA) under the Horizon Europe Framework Programme for Research and Innovation (2021 – 2027).

This deliverable (*First Progress Report 1 - M12*) has been prepared under the Work package WP1 – "*Management and Coordination*" of the FLAGCHIP project. In the context of WP1, the objective of D1.4 is to provide an overview of the non-sensitive activities performed in the first year of FLAGCHIP, including finished and ongoing activities. Many important developments took place in the first period (M1-M12), both from a technical perspective (i.e. Reliability models for SiC MOSFETS and UWBG, Public report of Packaging and Submodule Topologies and Public Report of the activities of C&HM) and a dissemination perspective, where the consortium is actively present and seeking synergies with stakeholders and other EU projects.

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List of Terms and Definitions

Table 1. Terms and Definitions

Abbreviation	Definition
PC	Project Coordinator
WGB	wide band-gap
UWGB	ultra wide band-gap
MVDC	Medium Voltage Direct Current
HVDC	High Voltage Direct Current
C&HM	condition and health monitoring
SiC	Silicon Carbide
RUL	Remaining Useful Lifetime
Ga_2O_3	Gallium Oxide
AlGaN	Aluminum Gallium Nitride
TCAD	Technology Computer-Aided Design
PCB	Printed Circuit Board

RTD	**Resistance Temperature Detector**
TSEP	**Temperature-Sensitive Electrical Parameter**
FBG	**Fiber Bragg Grating**
SCBG	**Scattering-Based Bragg Grating**
KPI	**Key Performance Indicator**
IPR	**Intellectual Property Rights**

1. Introduction

FLAGCHIP will validate wide band-gap (WBG) and ultra wide band-gap (UWBG) semiconductor technologies and their integration into more compact and cost-effective power modules, combining these developments with upgraded condition and health monitoring (C&HM) of power electronic components. To this end, the project activities will progress on the state of the art on 1) Power Modules, including innovations at device and package level; 2) Condition and Health Monitoring and 3) Cost Efficiency of the proposed solution and the system as a whole.

FLAGCHIP's approaches will be demonstrated through AC/DC and DC/DC applications at two strategically chosen pilot sites in France (DC/DC MVDC Converter) and Norway (AC/DC Offshore Wind Turbine and Substation Converter architecture). Therefore, these sites have been carefully selected to be complementary and represent the most relevant applications for power electronic, i.e. wind energy applications (including their generators and HVDC converter station) and MVDC converter based applications (linked to solar energy generation, electric vehicle charging or hybrid microgrids among other purposes).

FLAGCHIP main objectives are to make significant improvements in WBG and UWBG semiconductor technologies and leverage the advances to address critical challenges related to C&HM of power electronic components, with the focus on Renewable Energy Sources generation and DC grids applications. To this end, the project's overarching goal will be to develop technologies that will predict failures, facilitate predictive maintenance strategies, and provide more efficient, compact, and cost-effective solutions for power electronics. FLAGCHIP solutions will be showcased in scenarios involving AC/DC and DC/DC applications at two pilot sites. These sites have been thoughtfully selected to highlight their complementarity and relevance to the current landscape of the EU power electronics sector.

The specific goals that will enable the achievement of FLAGCHIP are presented hereinafter:

- To advance the state-of-the-art in temperature measurement and degradation estimation for WBG semiconductors, specifically targeting Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistors (SiC MOSFET) devices, ensuring a robust understanding of the devices' operational conditions and health status.
- To enhance the resilience and operational efficiency of power electronic systems through innovative C&HM methodologies based on the combination of data-driven and physics-of-failure approaches.
- To revolutionize current semiconductor technologies delving into innovative wide band gap and ultra-wide band gap power electronics.
- To develop the next-generation wide band gap power modules with increased performance, compact packaging and sensor integration.
- To carry out a complete validation and demonstration program of the project solutions up to TRL 5-6 in two different pilot sites.
- To achieve cost-effective integration, investigate into different costs models and carry out techno-economic models for the design of business models and service agreements for C&HM and maintenance.

- To ensure the exploitation of the project results by developing the corresponding business plans as well as their dissemination by reaching key stakeholders and promoting synergies with other R&D projects.

2. Explanation of the work carried out per WP

2.1 Work Package 1

The WP1 is dedicated to ensuring the effective coordination and overall management of the project, facilitating smooth collaboration among partners and maintaining communication with the European Commission. Its main objectives include applying sound management practices, ensuring the timely delivery of high-quality results in line with the Grant Agreement, monitoring financial aspects, evaluating performance, risks, and quality, and fostering innovation throughout the project duration. To date, 4 out of 11 deliverables related to WP1 have been submitted to the European Commission, including the Project Handbook, Data Management Plan first draft, Project Management Plan, and the RRI report. Furthermore, the milestone, M1 Project kick-off meeting, of the WP has been accomplished in M02.

The task related to the overall project management as well as overseeing the project's technical coordination**,** is led by CIRCE, the Project Coordinator (PC), who acts as the primary liaison with the European Commission. CIRCE as Project Coordinator manages the distribution of project funds in alignment with the Grant Agreement and Consortium Agreement and has implemented the project's governance structure. To support project collaboration, CIRCE established a SharePoint repository and a Teams channel, accompanied by a user guide to assist partners in using these tools efficiently.

The project monitoring and reporting task establishes the interim reporting process and the corresponding tool covering both technical and financial aspects. Monthly follow-up meeting, Steering Committee Board meetings are held quarterly, while four General Assembly meetings are scheduled biannually.

Regarding **quality assurance,** its process has been described in D1.1 “Project Handbook “and the review of each deliverable has been assigned to three different reviewers. Furthermore, the **Data Management Plan (DMP)** has been developed in order to ensure effective and compliant data handling throughout the project, in line with the constraints outlined in the Consortium Agreement and applicable data protection regulations. Ongoing oversight is being maintained to ensure adherence to the defined procedures for data storage, access, and use.

Last but not least, the works related to the **Responsible Research Innovation** of the project are focused on ensuring that project innovations are addressed from technical, regulatory, social, and organizational perspectives. All partners have been introduced to Responsible Research and Innovation (RRI) principles, covering public engagement, open access, gender, ethics, governance, and science education.

All Task Leaders and WP Leaders were actively involved in WP1, ensuring the timely and high-quality delivery of results, keeping track of all activities implemented within the individual tasks, participating in all project meetings and reporting their progress and efforts as per the CA obligations.

2.2 Work Package 2

The WP2 aims to advance the development of next-generation semiconductor devices for power electronics by designing improved wide bandgap (WBG) SiC-MOSFETs and exploring ultra-wide bandgap (UWBG) technologies such as Ga_2O_3, AlGaN, AlN, and diamond. The work will focus on reducing losses, enhancing short-circuit and surge current capabilities, and benchmarking new materials and devices for future power electronics applications. The WP includes the submission of 4 deliverables, with work continuing through month 30 of the project.

Over the last 12 months, our progress includes:

1) 3.3kV SiC-MOSFET reliability characterisation. The SiC-MOSFET used in WP2 is a 3.3kV device from Hitachi Energy. The current rating of each chip is about 25A. The same devices are used in a half -bridge 3.3kV 500A LinPak module manufactured by Hitachi Energy. In order to evaluate device reliability, a few reliability tests are carried out for both chips and power modules. First, the team of the University of Nottingham designed a TO-247-4L package for the die packaging. To carry out the tests, a half bridge electrical circuit was designed to measure switching transients waveforms, short-circuit robustness, overload turn-off switching and unclamped inductive switching. The PCB is shown in Figure 1.

Figure 1 : Dedicated PCB for dynamic switching tests for FLAGCHIP project

To evaluate the reliability of LinPak power module, an AC power cycling test bench was designed in Supergrid Institute, which allows the power cycling of the module at 250A and 2000V.

2) 3.3kV SiC-MOSFET reliability model. Technology Computer-Aided Design (TCAD) simulations are employed in FLAGCHIP to understand and predict the internal physics of SiC MOSFETs, and to support the development of reliable and optimised device designs. These models provide a physically grounded framework to assess performance and reliability under realistic operating conditions. The progress includes the interface and trap modelling, which reveals the performance of 4H-SiC MOSFETs affected by defects in the SiO_2 gate oxide and at the SiC/SiO_2 interface. We also developed a TCAD model for carrier mobility. As an example, good

agreement is shown between the TCAD model and the reference under different doping and temperature ranges in Figure 2.

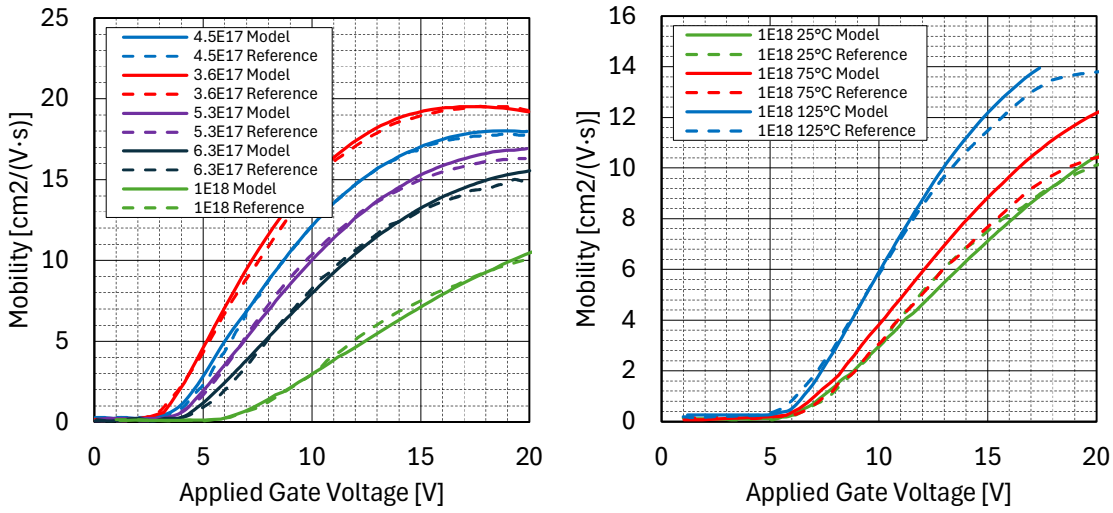

Figure 2 : Doping and Temperature Dependency of inversion layer mobility of TCAD model showing good predicting ability compared to reference values

3) 6.5kV SiC-MOSFET performance improvement. The progress of the activities carried out by mqSemi includes the development of a reference model in TCAD to benchmark 6.5kV SiC-MOSFET die developed in Hitachi Energy. mqSemi performed extensive TCAD simulation studies of a 6.5kV SiC MOSFET device based initially on a planar gate concept. The purpose of the simulations was to optimize the transistor cell size. As can be seen in Figure 3, there is an optimal transistor cell size for achieving a minimum on-state resistance value Rds-on. This is important in order to reduce the chip size and ensure the semiconductor costs are kept at a reasonable level. For transistor cells larger than this optimal value, there is a slight increase in Rds-on. Although this increase is not pronounced, a larger transistor cell size means that fewer cells can be packed in the same device area. This may be relevant for improving certain device operating criteria such as short circuit capability. For transistor cells smaller than the optimal value, there is a pronounced and rapid increase in Rds-on. The miniaturization of the semiconductor chip is not further possible based on a planar gate structure.

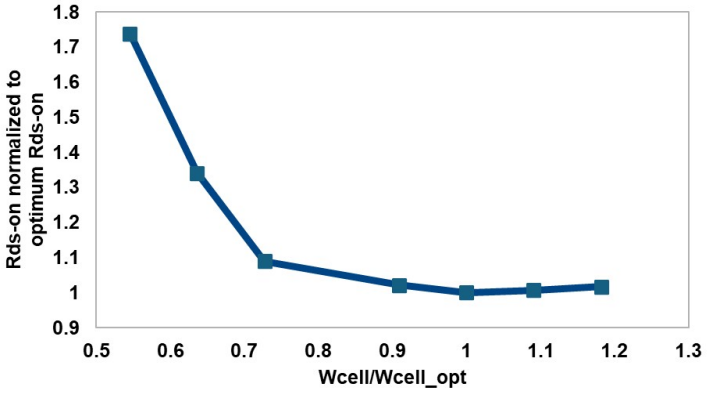

Figure 3 : Dependence of Rds-on vs. transistor cell size (Wcell) for 6.5kV SiC MOSFET (TCAD simulation)

In addition, mqSemi performed detailed simulations of the built-in diode of the SiC MOSFET. The reason for this study was the project goal of developing a SiC MOSFET chip with embedded temperature sensing capability. Detailed TCAD simulations were performed for a 6.5kV SiC MOSFET structure, and the Figure 4 shows clearly that as the junction temperature increases, there is a shift in the forward voltage drop across the diode (Vf).

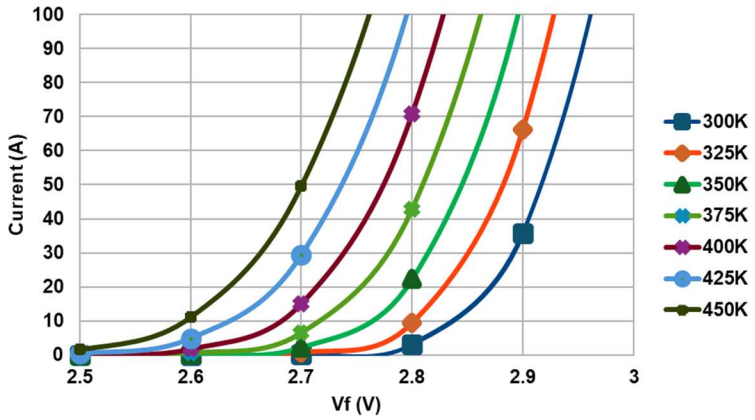

Figure 4: Static characteristic of the built in diode of 6.5kV SiC MOSFET (TCAD simulation) at nominal operating currents

A deliverable D2.2 that summaries the above work on SiC-MOSFET reliability characterisation and modelling has been submitted.

2.3 Work Package 3

The WP3 aims to develop innovative power module packaging and submodule topologies that enable improved thermal management, enhanced electrical insulation, and compact integration of advanced semiconductor devices. The work focuses on designing two sets of power modules (Type 1 and Type 2) optimized for medium-voltage applications, with enhanced cooling concepts and sensor integration to support condition and health monitoring. To date 1out of 7 deliverables related to WP3 have been submitted to the European Commission, so far (the “Specification document”). The WP will run until month 33 of the project.

A key aspect of this WP is the definition of technical and functional requirements for both module types. These requirements will take into account electrical ratings, mechanical constraints, thermal dissipation needs, and sensor integration strategies. Attention is paid to ensuring compliance with applicable international standards for high-voltage insulation and safety.

One of the core innovations to be explored is a new packaging architecture that integrates liquid dielectric cooling directly into the module. Dielectric fluids allow intended to simultaneously improve cooling efficiency and provide electrical insulation, replacing traditional encapsulants in the module. Various candidate fluids are examined in terms of thermal and dielectric properties, environmental impact, and compatibility with internal components. Experimental testing will support the selection process, complemented by fluid dynamics simulations to optimize flow and heat dissipation.

In terms of electrical design, the WP3 will introduce novel submodule topologies suitable for series connection of multiple high-voltage semiconductor devices. These topologies are to be optimized to

reduce parasitic effects and accommodate balancing circuits and protection elements. The layout and mechanical design consider the integration of sensors, driver circuits, and interconnection schemes in a compact form factor.

Sensor integration plays a critical role in enabling condition and health monitoring of the power modules. This WP assesses the feasibility of incorporating various sensing technologies, such as fiber-optic sensors (FBG and SCBG), temperature-sensitive electrical parameters, and conventional thermistors. The implementation strategy will cover sensor positioning, mechanical fixation, electrical interfaces, and insulation. Practical validation and calibration steps are to be performed to ensure the functionality and robustness of the sensing systems.

The final phase will focus on the manufacturing and validation of the two module types. Type 1 will feature the full set of innovations, including integrated cooling and sensor systems, while Type 2 will adopt a streamlined design with selected features based on performance and cost evaluations. Prior to deployment, the modules will undergo comprehensive testing—electrical, thermal, mechanical, and sensor-related—to ensure they meet the defined specifications and are suitable for integration into the project's pilot systems.

Overall, this WP will deliver the physical interface between semiconductor innovations and real-world applications, enabling the demonstration of FLAGCHIP technologies under demanding operational conditions.

2.4 Work Package 4

This WP focuses on the development of advanced condition and health monitoring (C&HM) solutions for power electronics, with the ultimate goal of increasing the reliability, efficiency, and operational lifetime of semiconductor devices and modules. It aims to identify the most accurate, cost-effective, and easily implementable monitoring techniques, as well as to define predictive models capable of estimating the remaining useful lifetime (RUL) of power modules. The activities will be carried out from month 4 until month 24 of the project and will result in 8 deliverables.

The first line of work will focus on exploring and validating multiple junction temperature estimation methods based on Temperature-Sensitive Electrical Parameters (TSEPs). These include techniques such as internal gate resistance measurement, on-state voltage (Vds,on) analysis, bandgap-based transducers, and Fibre Bragg Grating (FBG) optical sensing. Each method will be benchmarked in terms of accuracy, response time, integration complexity, and suitability for real-world converter operation.

Parallel efforts will concentrate on developing non-conventional health monitoring methods capable of detecting early signs of degradation in key module components, such as the semiconductor chips, bonding wires, and substrate interconnections. Measurement circuits and test routines will be designed to capture relevant indicators like voltage drift, strain, or thermal resistance variation, all of which will contribute to the diagnosis of component wear. . In relation to what has been described in WP2, measurement boards have been developed by SuperGrid to evaluate and decouple the parametric variations caused by temperature rise from those resulting from component ageing. This will enable a more precise and reliable CHM.

Another important activity will be the development of RUL prediction methods. The approach will rely on tracking the relative variation of electrical or thermal parameters over time, using simple extrapolation techniques to forecast when a device will reach its failure threshold. This strategy will avoid the need for complex models or intensive calibration, making it more flexible and applicable across different technologies.

To consolidate monitoring and predictive capabilities, a hardware platform—referred to as the health estimation monitor—will be developed and integrated at the gate-driver level. This platform will act as a real-time digital twin of the power module, emulating its expected behaviour and comparing it against live measurements to flag deviations indicative of incipient failure.

Additionally, control strategies will be designed to activate “limp mode” operation in power converters when predefined degradation thresholds are reached. This will allow systems to continue operating in a reduced-capacity mode, preventing sudden failures and ensuring safer operation. These strategies will be tested under representative use-case scenarios to verify their effectiveness in real operating environments.

In summary, this WP will bring forward innovative C&HM functionalities that will transform power modules from passive components into smart, self-monitoring systems. These developments will feed directly into other areas of the project, contributing to safer, more adaptive, and cost-efficient power electronic systems.

2.5 Work Package 5

This WP is dedicated to the demonstration, testing, and validation of the technological developments achieved throughout the project, with a particular focus on real-world performance under medium-voltage and offshore application conditions. The aim is to deploy and operate the innovative solutions developed—such as advanced power modules, monitoring systems, and control strategies—at two pilot sites and validate their performance against a defined set of technical and operational KPIs. The WP will run from month 17 until month 42 and will result in 6 deliverables.

The activities will begin with the definition of a comprehensive evaluation methodology, including technical, economic, and reliability-related indicators. These KPIs will serve as a reference to assess the progress and impact of the deployed solutions during pilot operation. They will be tailored to reflect the specific characteristics of the demonstration environments and the expected improvements in terms of efficiency, fault detection, thermal performance, and cost-effectiveness.

Once the evaluation framework is established, deployment activities will take place at the two selected pilot locations. One will focus on AC/DC converter architectures relevant to offshore wind applications, while the other will address DC/DC MVDC converters for grid integration and transmission systems. The new power modules, condition monitoring tools, and predictive control mechanisms will be integrated into existing testing infrastructures at these sites.

A key phase of the WP will involve the execution of a structured testing and validation campaign. This will include a pre-validation stage to ensure that all systems are correctly installed and functional, followed by extended operational trials under representative load conditions. Throughout these tests, data will be collected on the behaviour of the modules, including thermal stability,

sensor responsiveness, degradation progression, and the effectiveness of limp-mode strategies and RUL predictions.

Each pilot will maintain a detailed log of system performance, operational issues, and technical results. These logs will be used to evaluate the technologies against the predefined KPIs and identify potential areas for improvement. The results will also feed into feedback loops for fine-tuning of models, sensors, and control algorithms, as well as informing exploitation and scalability assessments.

All in all, this WP will validate the real-world performance and robustness of FLAGCHIP innovations, ensuring that the developed solutions are not only technically sound but also ready for application in demanding industrial scenarios. The insights gained through these demonstrations will be critical for assessing replicability and future deployment at a larger scale.

2.6 Work package 6

This WP focuses on supporting the cost-effective integration of FLAGCHIP innovations by developing models to assess and manage technical and economic risks associated with condition and health monitoring (C&HM), a strategy referred to as “stress steering.” The main objective is to enable smarter system design and informed business decisions by linking technical performance with economic outcomes. The WP will run from month 20 until month 42 and will result in three deliverables.

The first set of activities will focus on understanding the lifecycle cost of power semiconductor devices and related components. Using TCAD process simulations, the impact of key fabrication parameters—such as implantation profiles and thermal processing steps—on both performance and cost will be assessed. These insights will allow for the evaluation of cost-effective manufacturing paths for different device technologies, including SiC-MOSFETs of varying voltage ratings and UWBG devices. The cost of auxiliary components like sensors, packaging, and PCBs will also be considered, enabling a comprehensive cost assessment from the system designer’s perspective.

Building on this, simulation experiments will be used to demonstrate the cost-reduction potential of the FLAGCHIP innovations. These simulations will incorporate health monitoring data and remaining useful lifetime (RUL) estimations to optimize predictive maintenance strategies. Focused initially on offshore wind applications, the models will integrate operational factors such as failure risks, weather conditions, and logistical constraints to determine optimal maintenance scheduling at the wind farm level. This system-level approach will avoid sub-optimization by ensuring that decisions consider turbine interdependencies and resource planning.

The final stage of the WP will provide techno-economic models and long-term simulations to support the development of business models and service agreements for C&HM and predictive maintenance. These models will assess the profitability of implementing FLAGCHIP technologies over a full operational lifetime, , taking into account expected improvements in reliability and expected improvements in reliability and performance. The cost-benefit analysis will explore how economic risks and savings are distributed among stakeholders and how different contractual structures—such as performance-based maintenance agreements—could enhance adoption and reduce uncertainty.

In summary, this WP will provide the analytical foundation for translating technical advancements into economically viable and scalable solutions. Through lifecycle cost assessment, predictive maintenance modeling, and service agreement analysis, it will ensure that FLAGCHIP technologies are not only efficient and reliable but also financially sustainable in demanding applications such as offshore power systems.

2.7 Work package 7

WP7 is dedicated to the strategic dissemination, communication, and exploitation of the results generated throughout the FLAGCHIP project. This work package plays a pivotal role in ensuring that the project's innovations achieve maximum visibility, foster meaningful engagement with key stakeholders, and facilitate uptake beyond the lifetime of the project. Its overarching objective is to design, implement, and continuously refine a suite of targeted activities aimed at promoting FLAGCHIP's scientific and technological contributions across a broad and diverse audience—ranging from academia and industry to policymakers and standardization bodies.

To date, two key deliverables have been successfully submitted to the European Commission in alignment with WP7's objectives:

- D7.1: Dissemination and Communication Plan and Activities – outlining the strategic framework, tools, and channels employed to reach and engage target audiences;
- D7.4: Exploitation and Sustainability Plan – Initial Version – presenting a preliminary roadmap for valorising project outputs and securing long-term sustainability.

In addition, Milestone M2: Launch of the Dissemination, Communication, and Exploitation Plan, was successfully achieved in Month 6 (M6), marking the formal activation of WP7's operational agenda. This milestone confirmed the timely deployment of FLAGCHIP's outreach and impact strategies, ensuring coherence across project activities and alignment with Horizon Europe's key impact pathways.

During the first 13 months of the FLAGCHIP project, dissemination and communication activities have been strategically focused on raising awareness and effectively conveying the project's value propositions, overarching objectives, and key activities to a diverse range of target audiences. This foundational phase aimed to establish FLAGCHIP's visibility and credibility within the European research and innovation landscape, while also building momentum for stakeholder engagement and broader outreach. To guide these efforts, a comprehensive Dissemination and Communication Plan (DCP) was developed at an early stage of the project. The DCP outlines the strategic goals, target groups, communication tools, and performance indicators necessary to ensure a coherent and impactful approach. It is designed as a living document, subject to at least 2 updates to reflect project developments, stakeholder dynamics, and evolving dissemination opportunities.

Significant progress has already been made in operationalising the DCP. Notably:

- A coherent visual identity for the FLAGCHIP project has been created, encompassing logo design, templates, and graphic standards to ensure consistent branding across all communication materials and platforms.
- A suite of promotional materials—including a leaflet and a poster as well as slide decks—has been produced to support dissemination at events, conferences, and stakeholder meetings.

- An interactive project web portal has been launched, serving as a central hub for information dissemination, news updates, resource sharing, and stakeholder engagement.
- The project's social media presence (e.g., LinkedIn) has been actively maintained and regularly updated with curated content and multimedia, thereby fostering ongoing engagement with the broader community and increasing project visibility across digital channels.

During the first year of the project, two newsletters, 1 press release by Mitsubishi Electric, 13 online articles on the project's website, 1 technical publication, and 5 presentations at external events aimed to enhance our outreach to both academic and professional audiences.

Table 2. Communication tools and channels

Communication tools and channels	Link
LinkedIn	https://www.linkedin.com/company/flagchip-project/
Facebook	https://www.facebook.com/profile.php?id=61565428628434
X (Twitter)	https://x.com/Flagchipproject
Website	https://flagchip-project.eu/
News Items	https://flagchip-project.eu/news/
Newsletters	https://flagchip-project.eu/newsletters/
Promo Material	https://flagchip-project.eu/promotional-material/

Table 3. Events attended up to M12

What?	Where?	When?	Link
Forward Green Expo 2025	Thessaloniki, Greece	13-15.03.2025	https://flagchip-project.eu/flagchip-went-to-forward-green-2025/
IMB-CNM Talks: Energy Workshop II: Advancing Power Electronics for Efficiency	Online	14.3.2025	IMB-CNM Talks: Energy Workshop II: Advancing Power Electronics for Efficiency - YouTube
PCIM	Nuremberg, Germany	6-8.5.2025	https://flagchip-project.eu/flagchip-partners-shine-at-pcim-europe-2025/
TIGON workshop	Turku, Finland	27.5.2025	https://flagchip-project.eu/flagchip-featured-at-tigon/
ECCE Europe	Birmingham, UK	31.8-4.9.2025	https://flagchip-project.eu/flagchip-at-ecce-2025/

These efforts have laid a strong foundation for deepening stakeholder involvement in subsequent phases of the project. Looking ahead, the DCP will continue to evolve to support FLAGCHIP's transition from awareness-raising to more targeted engagement and impact-driven communication, in line with Horizon Europe's emphasis on openness, outreach, and long-term value creation.

In parallel, this WP aims to manage the knowledge emerging from FLAGCHIP, while planning for its protection and exploitation. For this purpose, an Innovation and IPR Management Strategy was defined in M6 to support the protection and responsible use of project-generated knowledge. A dedicated methodology was developed to guide the identification, documentation, and plan for the exploitation of FLAGCHIP's 18 Key Exploitable Results. All these were captured in an Exploitation and Sustainability Plan which includes exploitation routes, potential users, IPR provisions, and tailored action plans for individual and joint exploitation pathways.

Table 4. FLAGCHIP's Key Exploitable Results

#	Title
KER#1	WBG and UWBG devices TCAD and behavioural models to predict reliability
KER#2	New MOSFETs types
KER#3&4	Novel packages with integrated cooling and sensor in the power module
KER#5	Tj estimation based on TSEP
KER#6	Fiber Bragg Grating (FBG) sensors for Tj estimation
KER#7	Strategies and methodology for limp mode enabling
KER#8	RUL prediction model
KER#9	Power electronic digital twin for C&HM
KER#10	Costs Assessment, Cost-Benefit Analysis and Cost Models
KER#11	Wind farms maintenance optimization tool
KER#12	Techno-economic cost models for offshore wind farm maintenance
KER#13	Research data and scientific publications
KER#14	Lessons learnt and guidelines
KER#15	AC Power Cycling Results (Degradation)
KER#16	Innovative Test-bench (AC PCT with in-situ static parameters measurement (Vth, RDS_ON) with specific hardware
KER#17	TSEP vs DSEP (Reliable CHM)
KER#18	The integrated FLAGCHIP power module

Finally, targeted efforts have been undertaken to establish **strong synergies with other European initiatives,** recognising that collaboration beyond the consortium is essential for maximising impact, fostering knowledge exchange, and aligning with broader EU research and innovation strategies. These strategic interactions contribute to reinforcing FLAGCHIP's visibility and positioning within the **European power electronics ecosystem**.

As a first step, consortium partners carried out a **preliminary mapping and analysis of relevant initiatives (including the ones from the BRIDGE initiative)**, identifying projects and platforms with complementary objectives or technical relevance. Building on this groundwork, **Q-PLAN undertook the coordination of outreach activities**, including contacting project coordinators and DC leaders, facilitating bilateral meetings, and laying the foundation for meaningful synergies with interested parties.

By **Month 13 (M12)**, FLAGCHIP successfully established **six synergies** with European initiatives, namely: **HYNET**, **SAFEPOWER**, **MoWiLife**, **InterSCADA**, **AdvanSiC**, and **THEUS**. While the majority of these collaborations are currently focused on **joint dissemination and visibility-building**

activities (such as cross participation in events, promotion of each other's results through online means, etc.), they represent an important entry point for future technical collaboration.

Importantly, FLAGCHIP has joined a **project network titled "Grids projects" coordinated by the THEUS EU project**, which aims to foster structured collaboration and systematic knowledge exchange among EU-funded initiatives working in related domains. In this context, FLAGCHIP also recommended its sister projects, **SAFEPOWER** and **MoWiLife**, for inclusion in the network—leading to their subsequent invitation and participation.

All progress in this area will be systematically documented and reflected in future updates of the **Dissemination and Communication Plan (DCP) and the Exploitation and Sustainability Plan (ESP)**, ensuring that FLAGCHIP remains agile, outward-looking, and well-integrated within the EU R&I landscape.

3. Conclusions

During the first 13 months, significant progress was made across all Work Packages of the FLAGCHIP project, laying a strong foundation for the successful achievement of its objectives.

WP1 successfully ensured effective project coordination, management, and communication among partners and with the European Commission. Two out of ten deliverables were submitted, and one planned milestone was met. CIRCE, as Project Coordinator, established key project governance structures, tools, and reporting mechanisms. Responsible Research and Innovation principles were promoted, and the Data Management Plan was implemented to ensure compliant and secure data handling.

WP2 produced an AC power cycling test bench and a switching test board to test both the project 3.3kV SiC-MOSFET device and power module to understand their reliability. A 3.3kV SiC-MOSFET TCAD model has been developed to produce the reliability data such as the variation of channel mobility under different doping levels and temperatures. A TCAD structure model for 6.5kV SiC-MSOFET has been developed as a reference, which can be used to benchmark the improvement of device design in terms of device ON-state resistance, leakage current etc. in the future. A deliverable D2.2 reporting the up-to-date progress has been submitted.

WP3 produced a detailed specification document for the power modules, which is the stepping stone for the technological developments in WP3. Regarding Type 1 modules, an innovative a promising architecture has been identified, and is currently under investigation for IP protection. Several dielectric fluid candidates have been identified, purchased, and are currently under test. A first set of 6.5kV SiC MOSFET has been delivered by HITACHI. Regarding Type 2 modules, it was found that the initial project schedule, in which modules were to be delivered by M33 was unsuitable for some of the work carried in WP2 and 4. As a consequence, a set of Type 2 modules with limited changes was produced and delivered to MERCE, SUPERGRID and UoN by HITACHI ahead of schedule.

WP4 produced a detailed specification document for the power modules, which is the stepping stone for the technological developments in WP3. Regarding Type 1 modules, an innovative a promising architecture has been identified, and is currently under investigation for IP protection. Several dielectric fluid candidates have been identified, purchased, and are currently under test. A first set of 6.5kV SiC MOSFET has been delivered by HITACHI. Regarding Type 2 modules, it was found that the initial project schedule, in which modules were to be delivered by M33 was unsuitable for some of the work carried in WP2 and 4. As a consequence, A set of Type 2 modules with limited changes was produced and delivered by HITACHI ahead of schedule.

WP5 has not yet started but the work carried out in WP2 and WP4 provide confidence in the progress achieved so far and in the future activities of WP5.

WP6 is not starting its activities before month 20. But to prepare, WP6 partners have, during the first 12 months, been following development in the other technical WPs and mapped interdependencies with other project activities as well as potential synergies with other projects.

WP7 successfully addressed the early stages of dissemination, communication, and exploitation within the FLAGCHIP project. Two deliverables have been submitted to the European Commission,

namely the Dissemination and Communication Plan and the initial Exploitation and Sustainability Plan. The key milestone M2 was achieved in M6. Over the course of the first 13 months, a wide range of activities were implemented to set the ground for the efficient and meaningful promotion of the project including the development of a visual identity, promotional materials, an interactive web portal, and a consistently active social media presence. In its first year, the project released 2 newsletters, a press release by Mitsubishi Electrics, 13 online articles, one technical publication, and participated at five external events. An Innovation and IPR Management Strategy was also established, along with a dedicated methodology to support the identification and facilitate the exploitation of FLAGCHIP's 18 Key Exploitable Results (as perceived at this stage of the project). Finally, FLAGCHIP has made considerable efforts in building open communication pathways with key relevant initiatives and actions such as EUREC, Enlit, MoWiLife, SAFEPOWER, InterSCADA, THEUS, HYNET, AdvanSiC, and others.

Overall, the project has demonstrated strong alignment with its technical, managerial, and dissemination goals. The foundations laid during these 13 months provide a solid foundation for the upcoming work and the achievement of FLAGCHIP's long-term impacts.

FLAGCHIP

FLAGSHIP SOLUTIONS IN POWER ELECTRONICS

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