# On-chip Temperature Measurement Using Fibre Bragg Grating Sensors with Thermal Network

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## Abstract

Fibre Bragg Grating (FBG) sensors are an emerging technology in the topic of power semiconductor condition monitoring, providing rapid and accurate measurement of junction temperatures. Typical temperature-sensitive electric parameters often require complex measurement circuitry and may vary with device ageing. FBG sensors can be physically interfaced with dies, are immune to electromagnetic interference, and will not vary in response as devices age. This paper provides an overview of the use of FBG sensors for on-chip temperature measurement under power cycling, evaluates the transient response, and demonstrates how a simple lumped RC thermal network can be used to improve measurement accuracy.

## 1 Introduction

With the push towards higher operating temperatures and faster switching speeds offered by wide band-gap devices (WBG) such as silicon carbide (SiC) or gallium nitride (GaN), it becomes ever more crucial to provide accurate lifetime estimation. Consequently, rapid and precise estimation of the device junction temperature ($T_j$) is critical for condition and health monitoring platforms which aim to prevent costly downtime of critical and expensive systems and facilitate preventative maintenance. Estimation of device remaining useful life is commonly performed with temperature-sensitive electric parameters (TSEPs), which are at-the-terminal measurable device parameters that vary with device temperature [1]. However, these parameters often require calibration in conjunction with complex measurement circuitry, are not device technology (Si, SiC, GaN) agnostic [2], and in some cases have been demonstrated to vary with advanced ageing of the device [3], [4].

An approach for mitigating TSEP variation with ageing using online recalibration has been demonstrated recently [5], but this is currently only shown for a single TSEP and only for SiC-MOSFETs. It should be noted that the temperature profile across the semiconductor die is not uniform during heating. TSEPs can only give an average estimate of the junction temperature and cannot provide information sufficient to describe the non-uniform heating. Alternate methods of $T_j$ estimation have been studied, such as the use of thermal imaging and die-embedded temperature-sensitive diodes [2], [6], but these are not yet proven in field operation and may not always be suitable for integration into the device packaging structure.

In this work, semiconductor die temperature measurement based on an emerging method of using fibre Bragg grating (FBG) sensors is presented. Compared to TSEPs, FBG sensors have simple calibration procedures and are immune to electromagnetic interference [7]. They are also capable of continuous temperature measurement through the commutation interval, limited only by the integration time of the interrogator. This is an advantage over some commonly used TSEPs that require measurement using current injection during turn-off [8].

Other physical contact sensors such as thermocouples are often electrically conductive and are hence unsuitable for on-chip measurement. In our previous work, the feasibility of using FBG has been demonstrated by measuring die temperatures during power cycling [9]. Transient temperature measurement error was evaluated, and a method of removing the FBG jacket to reduce the error was demonstrated. A limitation of that work was the fragility of the altered fibres, hindering applicability to real-world installations.

Recent studies have succeeded in using distributed FBGs within the baseplate of power modules positioned underneath the chips [10], or integrated within press-pack IGBT modules [11]. These single-fibre multipoint measurements highlight a key advantage of FBGs over tip-interfacing optical temperature sensors, which measure only a single point with each fibre [12]. In a similar manner, the use of TSEPs for a module packaged with multiple dies in parallel provides limited information for the behaviour of each individual die, only an average value.

As the diameter of the sensor cladding and jacket is small, any time-lag between die heating and FBG core heating should be negligible. However, the interface of the FBG and die is still of critical importance, as demonstrated by other researchers investigating silicone gel or thermally conductive adhesive contacts [13], [14] used to reduce temperature measurement error arising from a marginal air gap between the die and the sensor. However, the longevity of the thermal adhesive is not yet studied, and its use may introduce additional confounding factors such as the introduction of strain components arising from degradation of the bond interface.

This work proposes a non-invasive correction method based on a simple RC lumped thermal network to improve the accuracy of the sensor temperature measurement. The approach highlights a significant step towards a workable solution for the future integration of FBG sensors into power electronics module (PEM) packages and provides further practical insight into the use of FBGs for $T_j$ measurement directly from the semiconductor chip.

The paper is structured as follows. An overview of the theory and operation of FBGs is first provided, followed by experimental evaluation of the uncorrected transient response of FBGs under power cycling. The lumped RC network is then introduced alongside a method to determine the model parameters, which is used to correct the transient response. The model is then validated through additional power cycling experiments with different heating currents. Finally, the method is compared to a similar lumped RC network containing no FBG component to highlight the benefit of its inclusion.

## 2 Fibre Bragg Grating Temperature Sensors

FBG sensors are created from optical fibres by the uniform inscription of a Bragg grating array within the fibre core. This periodic grating modulates the core's refractive index, creating a localised selective filter which reflects a particular wavelength of incident light (1) [13], [15]:

$$\lambda_B = 2 \cdot \Lambda \cdot n_{eff} \tag{1}$$

where $\lambda_B$ is the reflected (Bragg) wavelength, $\Lambda$ is the period of the grating, and $n_{\text{eff}}$ is the fibre's effective refractive index.

This wavelength is sensitive to changes in temperature ($\Delta T$) and strain ($\Delta\varepsilon$) about the grating, allowing its use as a temperature or strain sensor (2):

$$\frac{\Delta\lambda_B}{\lambda_B} = \Delta T(\alpha + \xi) + \Delta\varepsilon\left(1 - p_{eff}\right) \tag{2}$$

where $\Delta\lambda_B$ is the wavelength variation, $\alpha$ is the thermal expansion coefficient of the fibre, $\xi$ is the thermo-optic coefficient of the fibre, and $p_{eff}$ is the photo-elastic constant for the fibre.

In strain-free or constant strain arrangements (i.e. $\Delta\varepsilon = 0$), the reflected wavelength varies only with temperature [7]. **Figure 1** illustrates the typical structure and behaviour of an FBG sensor, with the red lines representing laser inscriptions in the fibre made to adjust the refractive index. A full single FBG sensing head with grating width $W$ is made up of multiple inscriptions, spaced apart with periodicity $\Lambda$. Typical sensitivities of FBG sensors are reported around 10–14 pm/°C [10], [16].

The mapping between reflected wavelength and temperature ($\lambda - T$) is easily found through a procedure of stepwise heating of the fibre using a programmable temperature chamber or precision hot plate. At each temperature interval the corresponding wavelength is recorded, and the resultant data are fit to an appropriate model.

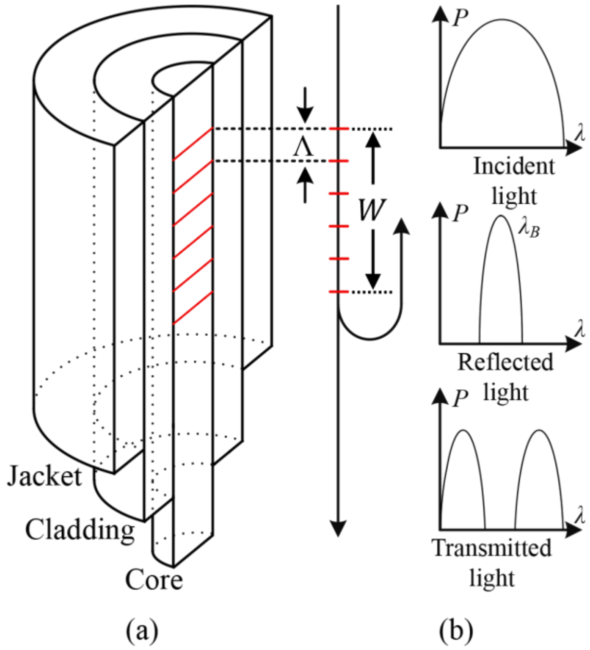


**Figure 1** FBG sensor (a) construction cross section showing grating inscriptions with period $\Lambda$ and total grating width $W$ for one sensor, (b) amplitude-wavelength light propagation dynamics.

This work uses the quadratic temperature-wavelength mapping model demonstrated in [14] (3):

$$T_{FBG} = p_1 + p_2 \cdot (\lambda - \lambda_B) - p_3 \cdot (\lambda - \lambda_B)^2 \tag{3}$$

where $T_{FBG}$ is the interpreted FBG temperature reading, $\lambda$ is the measured wavelength, and $p_i$ are polynomial fitting coefficients ($i = 1, 2, 3$).

A linear model with only two polynomial fitting coefficients is also commonly used, but the quadratic model is selected here due to a slightly higher $R^2_{adj}$ after fitting.

**Figure 2** shows several calibration results for a single FBG sensor with fits determined using (3).

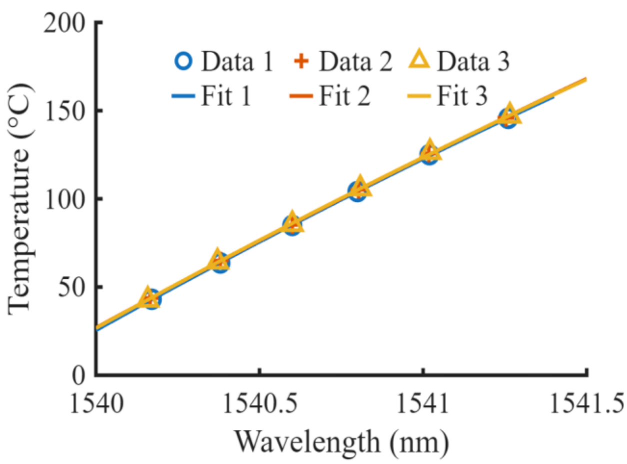


**Figure 2** FBG sensor ($\lambda_B = 1540$ nm) calibration results over three runs.

# 3 Temperature Measurement Under Power Cycling

## 3.1 Test Vehicle and Method

The performance of the FBG sensor is evaluated through a power cycling application. For this purpose, a simple silicon diode soldered to an active metal brazed aluminium nitride substrate is chosen. Electrical contacts are made with aluminium wire bonds.

To ensure a strain-free configuration of the FBG sensor, it is affixed using Kapton tape at only one side, with the fibre raised to the height of the die. The fibres selected for this work contained FBG sensors with $\lambda_B = 1540\,nm$ and a grating width of 3 mm.

In any device, the heating is not perfectly uniform, and a thermal contour across the die surface may be present during power cycling. For this test vehicle, the greatest temperature swings were observed in the centre of the die using a mid-wave infra-red (MWIR) thermal camera (CEDIP Titanium), which was chosen as the location for the sensor. The die surface is painted matte black to facilitate the thermal imaging. **Figure 3** shows a photograph of the test vehicle used in this work, in situ of the power cycling equipment and with the FBG sensor attached.

The test vehicle is placed into bespoke power cycling equipment and subjected to constant current cycles to cause heating and cooling. The die surface temperature is recorded using a MWIR camera during cycling and used as a baseline to evaluate the interpreted FBG response. Pyrometers held above the samples provide a constant temperature measurement to the power cycling equipment, allowing for a cycling regime with fixed temperature bounds of 40–90 °C to suit the single integration time setting of the MWIR camera.

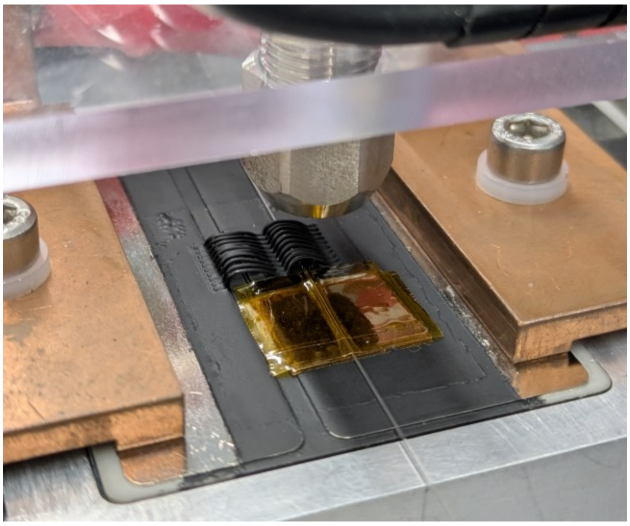

**Figure 3** Photograph of Si-diode test vehicle in situ of power cycling equipment, fibre laid flat across the die with FBG sensor situated in the centre.

## 3.2 Transient Response During Power Cycling

Power cycling trials with varying heating currents were performed to investigate the FBG response. **Figure 4** shows the chip and interpreted FBG temperature records for a single cycle at 40 A. Records are taken with stable temperatures, after a few minutes of the fixed-temperature cycling.

During the heating portion, a significant temperature measurement error is present in the interpreted FBG result. This is similar to the result for such arrangements observed by other authors [7], wherein it was attributed to the existence of an unavoidable airgap between the chip surface and the FBG sensor. Although it is possible to reduce this error using a thermal interface material, these approaches have untested long-term viability and may pose difficulty for integration into PEMs at the assembly stage or as a retrofit.

Our previous work demonstrated an approach for on-chip FBG temperature measurement correction where the jacket of the fibre is removed to reduce the distance between the fibre core and the chip [9]. In practice, the jacket provides most of the flexural strength of the fibres, and the altered fibres were found to be too fragile for most practical applications. Consequently, there arises the opportunity for additional solutions which preclude these limiting factors. One such is the use of a parameterised RC thermal network to correct the FBG sensor reading.

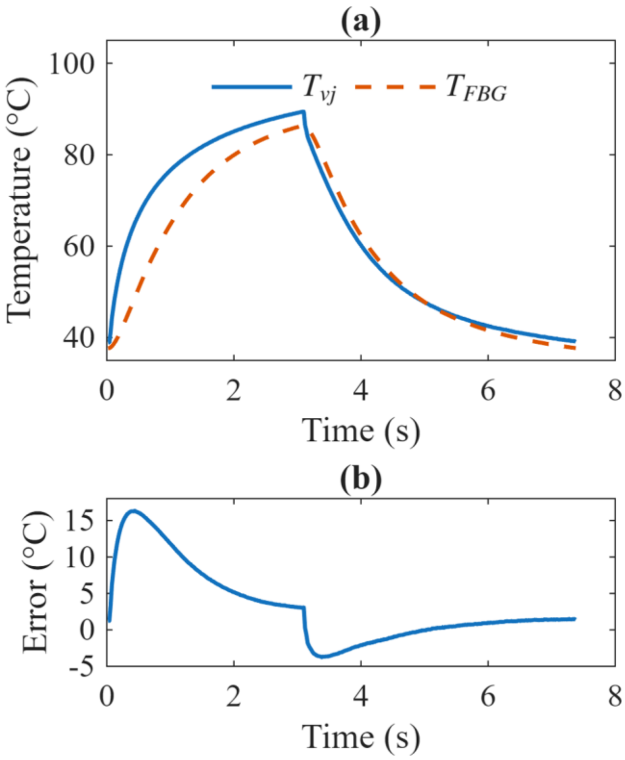


**Figure 4** Temperature records (a) under power cycling at 40 A using infra-red imaging of die surface ($T_{vj}$) and interpreted FBG response ($T_{FBG}$), (b) error between FBG and MWIR.

# 4 Error Mitigation Using Sensor Thermal Network

A simple lumped RC network can be used to represent the thermal resistances and capacitances of the system, as shown in **Figure 5**. The duration of simulations of this model performed in LTspice scaled with the number of RC cells, with more cells significantly increasing the computation effort. The error was not observed to reduce for the added computation time past the case with three cells; representing the FBG jacket, cladding and a possible airgap between the sensor and the die; and five for the diode coupon representing the thermal pathway from the die into the cold plate. Estimated power loss derived from measured voltage and current provides a heat source in the model, represented by **I1**. The FBG-recorded temperature is modelled via **V1**, the coolant temperature of 25 °C by **V2**, and the junction temperature estimate is measured at node **A**. Due to the lumped nature of the model, convection effects are implicitly included. The RC cell parameter optimisation procedure is demonstrated diagrammatically in **Figure 6**. This shows how the FBG measurement and power loss estimates are input to the model, which provides the junction temperature estimation for that set of RC values. The estimated temperature is compared with the MWIR baseline to find the error, which is minimised by the optimisation loop in MATLAB to provide a new set of RC values, which then calls LTspice to simulate the netlist using the new parameter set. This process repeats until the optimal RC parameters are found.

**Figure 7** shows the thermal network correction results for power cycling at 60 A after the optimisation procedure. The approach is shown to reduce the maximum temperature measurement error in the FBG response from 27.76 °C down to 2.13 °C. This demonstrates the possibility of easy correction of the FBG measurement inclusive of convection and any slight air gap between the die and sensor. Once the model parameters are determined, additional correction is performed with only changes in the input power loss and uncorrected FBG reading required.

To further evaluate the robustness of the model and general applicability of the approach, power cycling experiments were carried out at higher currents to retrieve additional model parameter sets. Each calibrated model was then validated against the rest in a round-robin format to identify any underlying trends or weaknesses.

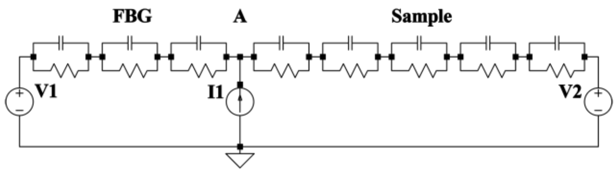


**Figure 5** RC thermal network representing the FBG sensor (left side) and diode coupon (right side). Power loss in die represented by **I1**, FBG temperature reading by **V1** and coolant temperature (25 °C) by **V2**, node **A** represents the model-corrected FBG temperature.

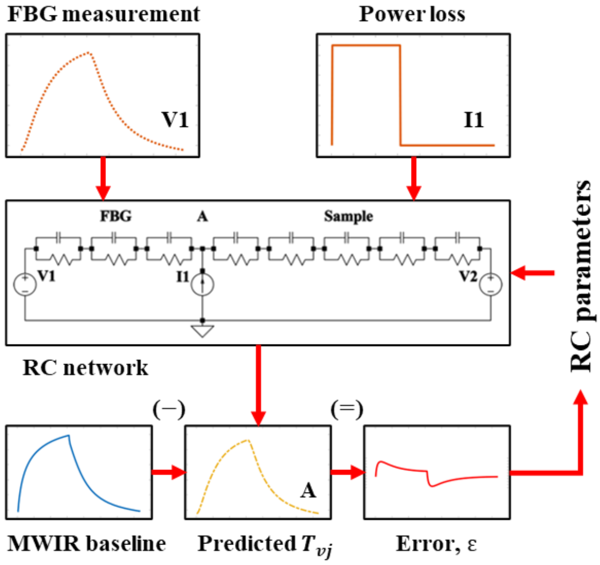


**Figure 6** RC cell parameter optimisation procedure controlled by MATLAB iteratively running LTspice simulations.

To demonstrate the capability of the method to correct FBG temperature estimates at a range of heating currents, **Figure 8** presents interpreted temperature records using a model calibrated at 60 A when applied to power cycling at 50 A and 55 A. It is shown that for both cases, the temperature measurement error is significantly reduced when the model is applied.

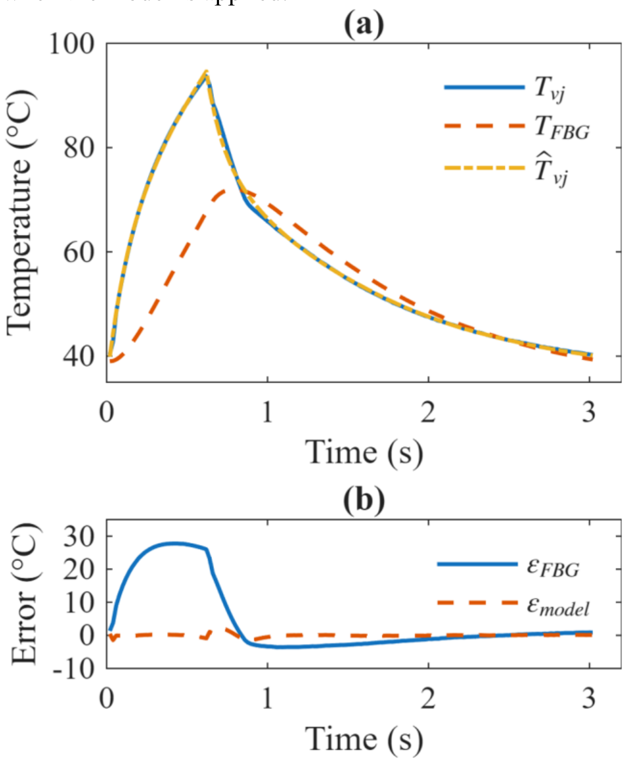


**Figure 7** Thermal network correction results for FBG reading under power cycling at 60 A. (a) MWIR temperature baseline ($T_{vj}$), uncorrected FBG temperature reading ($T_{FBG}$), model-corrected FBG reading ($\hat{T}_{vj}$), (b) error between baseline and uncorrected FBG reading ($\varepsilon_{FBG}$), error between baseline and model-corrected FBG reading ($\varepsilon_{model}$).

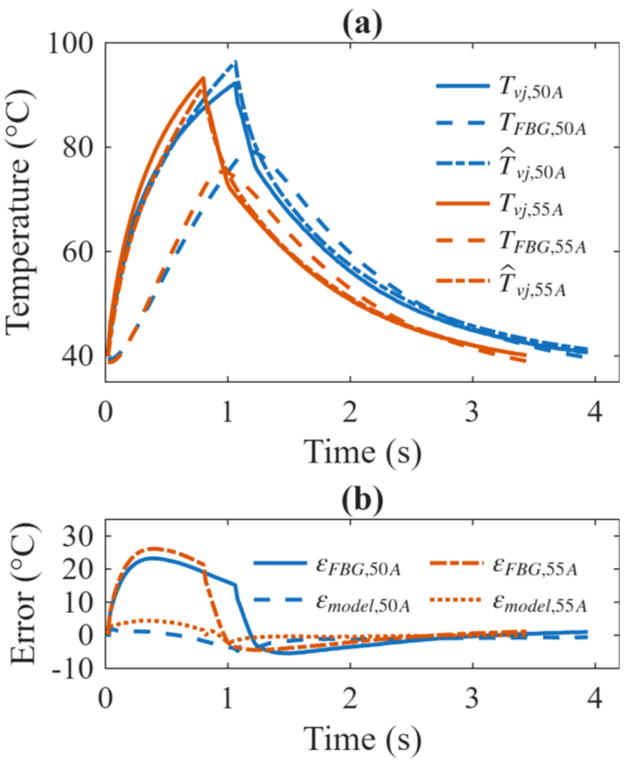


**Figure 8** Comparison of model-corrected FBG readings using 60 A model independently applied to 50 A (blue) and 55 A (orange) power cycling. (a) temperature records, (b) errors between baseline and model-corrected estimates.

The maximum temperature measurement errors for each calibrated model against each validation scenario are provided in **Table I**. Excluding the results where the same calibration and validation currents are used it is shown that the model is most accurate when the calibration and validation currents are close together. In general, the model with parameters determined at the highest calibration current (60 A) provided the lowest overall maximum temperature errors. In every case, the maximum error before and after correction was found during the heating portion of the power cycling test. Consequently, the calibration should be tailored to the specific application requirements, but with a weighting towards the higher side of the current demand. Nevertheless, these results highlight a promising, easy-to-develop correction procedure for on-chip temperature measurement using FBG sensors.

TABLE I
MODEL-CORRECTED FBG TEMPERATURE ESTIMATE ERRORS FOR VARIED HEATING CURRENTS

| Calibration current (A) | Max error at validation current (°C) | | | | |
|---|---|---|---|---|---|
| | 40 A | 45 A | 50 A | 55 A | 60 A |
| 40 | — | 6.80 | 8.85 | 12.25 | 11.63 |
| 45 | 10.66 | — | 5.87 | 12.37 | 12.07 |
| 50 | 11.88 | 7.40 | — | 6.40 | 6.64 |
| 55 | 14.15 | 11.80 | 7.88 | — | 6.16 |
| 60 | 9.84 | 7.90 | 4.79 | 4.40 | — |

# 5 Comparison of Performance Against no-FBG Network

The thermal network requires an accurate estimation of the heat generated by the die during conduction, which is obtained via voltage and current measurements to provide power loss. It is possible to construct a thermal model containing no FBG components and follow the same procedure with no additional complexity arising from the inclusion of the FBG sensor. The question arises as to whether the simpler model is as effective a tool to predict the die temperature when compared to the case including FBG elements. To address this, the same temperature data were used in the optimisation procedure with an RC network having only cells corresponding to the layers of the sample. This model contained no FBG RC-cells, and no FBG temperature measurement reference was used.

For a calibration performed at 60 A, the baseline and estimated values for die temperature under power cycling at 55 A are shown in **Figure 9**. The model-corrected FBG measurement for the same power cycling test is also included, for demonstration purposes. This result provides a maximum temperature measurement error of 9.73 °C, compared to 4.40 °C for the case including the FBG components. The no-FBG model diverges from the baseline during the cooling phase, whereas the model including FBG components does not.

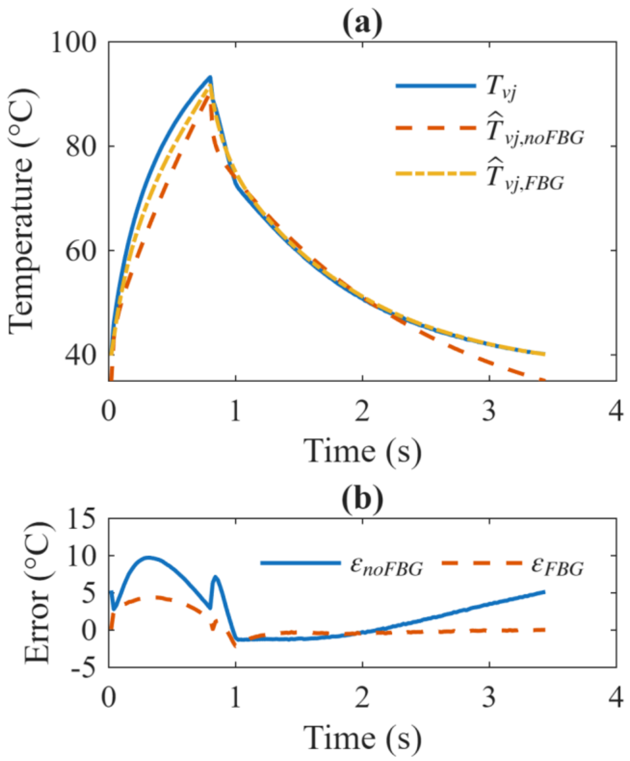


**Figure 9** Comparison of RC network based temperature estimation with and without FBG included in the model, power cycling at 55 A using model parameterised at 60 A. (a) die surface baseline ($T_{vj}$), no-FBG model-corrected estimate ($\hat{T}_{vj,noFBG}$), FBG model-corrected estimate ($\hat{T}_{vj,FBG}$), (b) errors between no-FBG estimate and baseline ($\varepsilon_{noFBG}$) and between FBG estimate and baseline ($\varepsilon_{FBG}$).

To further outline the advantage of the FBG-inclusive model over the simpler model, the same round-robin calibration-validation procedure was conducted for the no-FBG case. These results are provided in **Table II**, showing that for almost every combination of model calibration and validation current, the FBG-inclusive model provides a better estimation of the junction temperature compared to the no-FBG model.

A typical approach for calibration of these models is to use the step response, attempting to expose all time constants within the system: high frequency components from the pulse edge and low frequency components from the infinite settling time. In practice this is limited by the non-instantaneous power transition at the rising edge, and the infeasibility of waiting for infinite settling time. This study chose to use the fixed-temperature power cycling regime as a basis for both calibration and validation for ease and practicality, and consequently the resultant temperature pulses do not capture all system time constants. This could contribute to the result where better fits are found when the calibration and validation datasets use similar heating currents, and poorer fits are shown when currents are wider apart, as the exposed system time constants in each scenario may not align as well.

A portion of the error for the no-FBG model must also be attributed to the fact that the die temperature baseline is taken from the hottest spot of the die (in the centre) using MWIR thermal imaging. Modelling using power loss alone gives only an estimate of the average die temperature, in a manner similar to TSEPs, whereas the FBG temperature sensor can be precisely positioned to provide an accurate measurement of the hottest portion of the die.

# 6 Conclusion and Perspectives

In this work, a simple RC thermal network is proposed to correct temperature measurement error from FBG sensors applied directly to a power semiconductor chip surface, aiming to provide accurate and precise hot-spot temperature estimation. The test vehicle used was a silicon diode coupon, with aluminium wire bonds and soldered to an AlN AMB substrate, taken as a representative case for the major constituents of a PEM and subjected to fixed-temperature power cycling with bounds 40–90 °C. Parameterisation of the RC network is performed through an optimisation procedure using MATLAB to call LTspice, minimising error between the corrected FBG measurement and a baseline measurement recorded using MWIR thermal imaging.

The presented method is shown to reduce the FBG temperature measurement error under power cycling by 6.48–21.74 °C with a model parameterised at 60 A, depending on the heating current used for cycling. A study of the model robustness is carried out for different permutations of calibration and validation currents, revealing that the approach works best when calibrated at a current similar to the target application with a slight bias towards higher-current calibration.

TABLE II

NO-FBG TEMPERATURE ESTIMATE ERRORS FOR VARIED HEATING CURRENTS

| Calibration current (A) | Max error at validation current (°C) | | | | |
|---|---|---|---|---|---|
| | 40 A | 45 A | 50 A | 55 A | 60 A |
| 40 | — | 10.53 | 13.25 | 19.73 | 15.01 |
| 45 | 10.61 | — | 5.03 | 13.13 | 8.00 |
| 50 | 18.70 | 11.69 | — | 17.58 | 17.60 |
| 55 | 31.37 | 21.18 | 13.57 | — | 12.20 |
| 60 | 29.77 | 19.40 | 9.84 | 9.73 | — |

As the proposed method requires measurement of voltage and current to estimate the power loss in the chip to provide heating loss in the model, a comparison was made with a different model which depends only on these measured parameters. Through the same model robustness study, it is found that in almost every combination of calibration and validation current, the model including FBG provides a better estimate of the junction temperature. This highlights the model-corrected FBG measurement method as a feasible alternative to TSEPs, and to other contact-based measurement approaches.

A major advantage of the FBG sensor is its quasi-distributed capabilities, where multiple individual sensing heads are inscribed into a single optical fibre utilising wavelength division multiplexing [10]. Here, each sensor reflects a unique particular Bragg wavelength ($\lambda_B$), which could be applied to individual chips to provide a more precise insight into the module's behaviours. Future work will demonstrate how the approaches laid out in this work can be applied to a system consisting of multiple dies to provide individual temperature estimates, as well as provide a direct comparison between FBG- and TSEP-based $T_j$ estimates.

The contact between the fibre and the die is still an important consideration, which is not addressed in this work, especially considering a module potted with silicone gel. Detailed investigations into the longevity of the thermal interface adhesives and gel-bonding approaches as shown by other authors will be performed, in order to provide additional insight into the practical application of FBG sensors for on-chip temperature measurement.

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